GenRad

GR2225/PSF
Schematic Diagrams

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0100-010

GenRad, Inc. ☐ Service Products Division ☐ 4620 N. 16th Street ☐ P.O.Box 32295 ☐ Phoenix, Arizona 85064 ☐ TWX 910-957-4589 ☐ (602) 264-2475

Geography
Cartographic Diagrams

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GR2225/PSP Schematic Diagrams

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Customer Update

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Name and Title: _____

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Phone: _____

Equipment Purchased:

Model No. _____

Serial No. _____

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THIS END UP

GR2225/PSP
Schematic Diagrams

PSP SCHEMATICS

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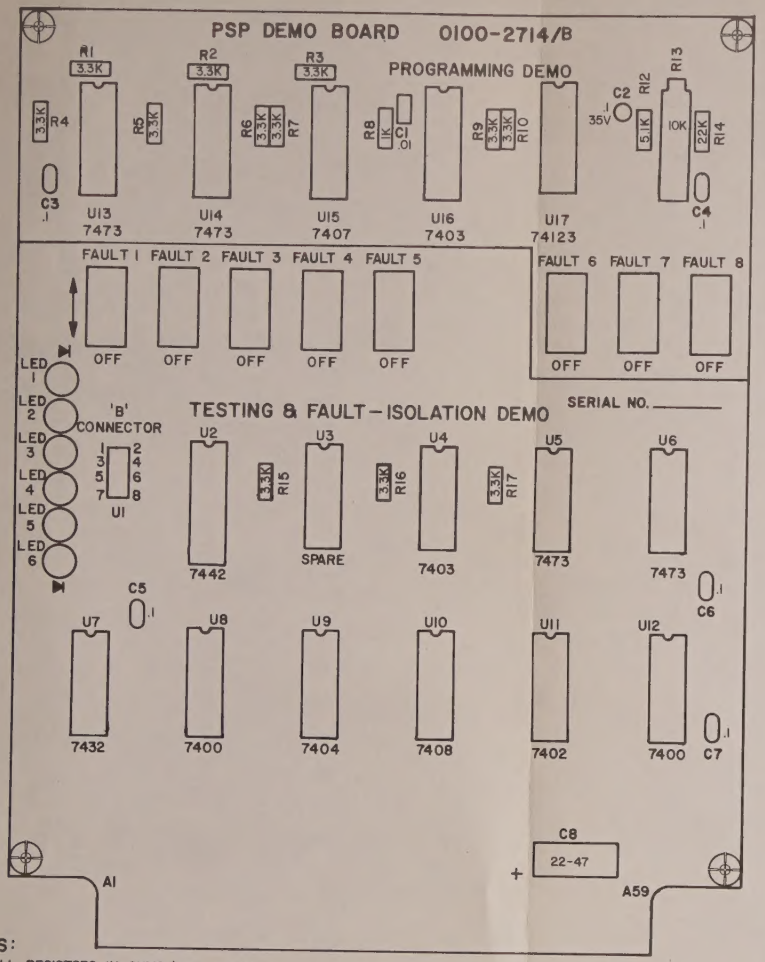
REVISION				
ISSUE	REL/CN NO	DATE	APPD	DESCRIPTION
A		3-15-78	JLW	REVISED PER DEBUG
B		6-14-78	DRS	REVISED PER ECO 112
—		12-10-79	DRS	REDRAWN WITHOUT CHANGE



NOTES:
1. ALL RESISTORS IN OHMS ±5%, 1/4 W.
2. ALL CAPACITORS ARE IN MICROFARADS.

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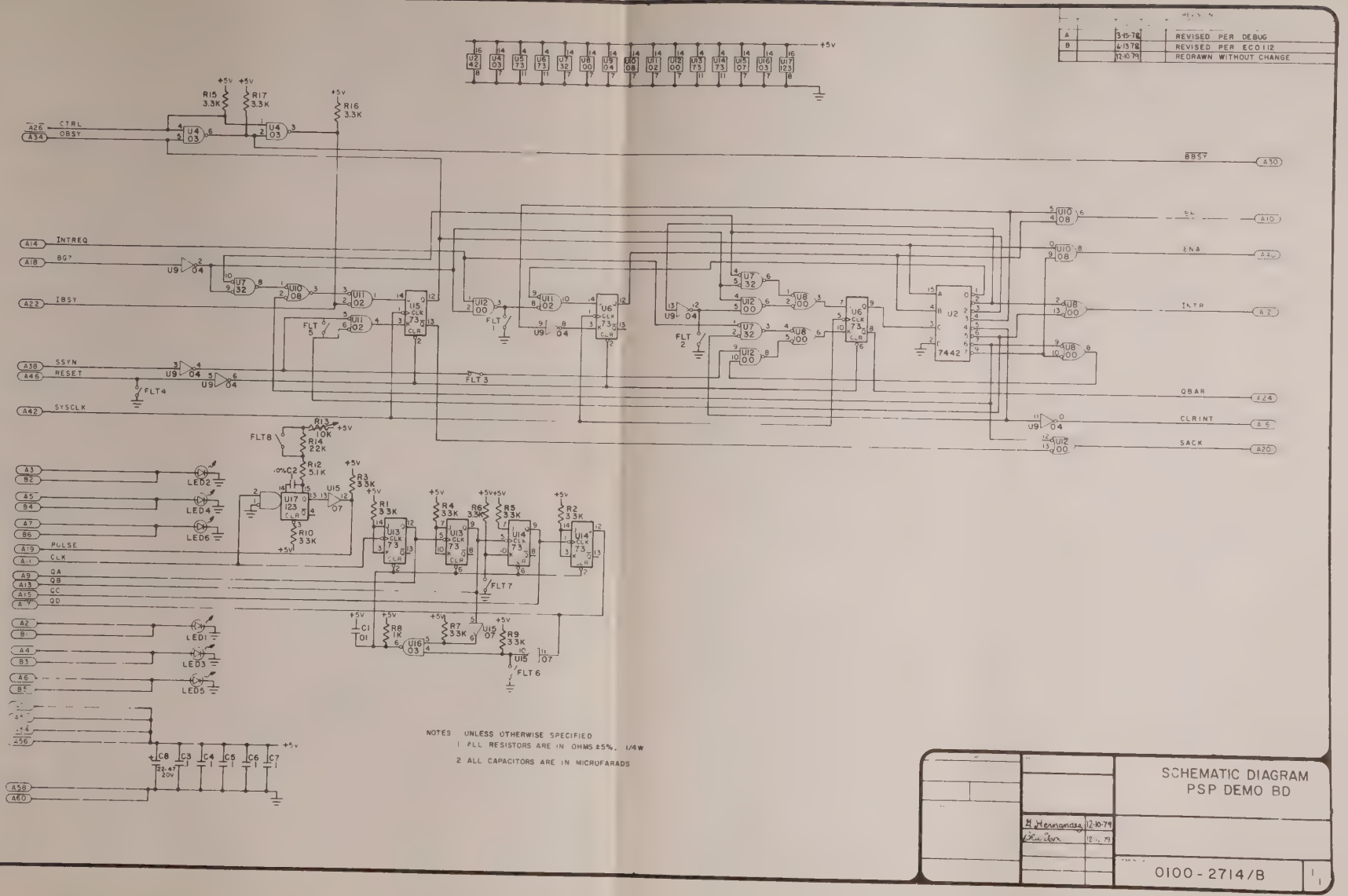
DRAWN BY	SILER	DATE 12-10-79
ENGINEER		DATE 5-10-73
DESIGN MANAGER		DATE

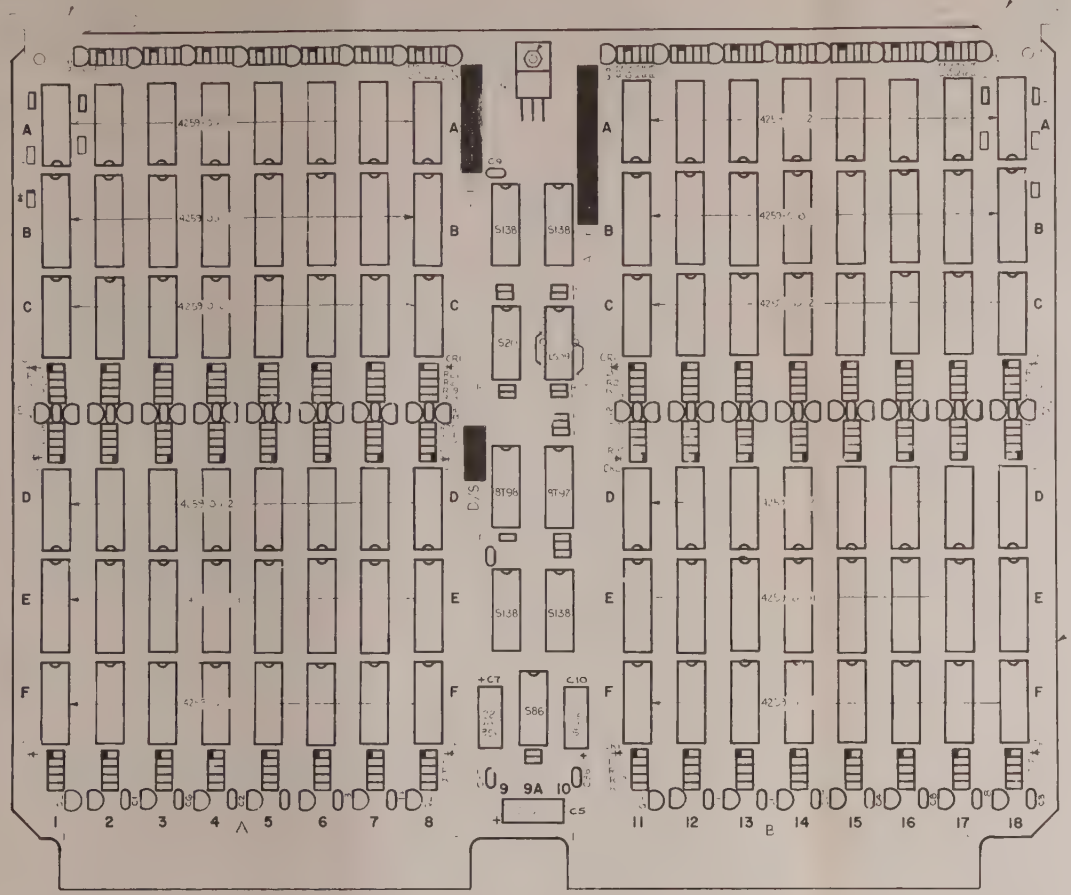
TITLE: CIRCUIT CARD ASSEMBLY
PSP DEMO BD

PHOENIX ARIZONA 85018

DRAWING NO. 0100-2714/B

SHT 1/1


REVISED PER DEBUG
REVISED PER ECO 112
REDRAWN WITHOUT CHANGE
SCHEMATIC DIAGRAM
PSP DEMO BD
0100-2714/B
M. Hernandez 12-10-79
NOTES UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE IN OHMS ±5%, 1/4W
2 ALL CAPACITORS ARE IN MICROFARADS
CTRL
OBSY
INTREQ
BG7
IBSY
SSYN
RESET
SYSCLK
PULSE
CLK
QA
QB
QC
QD
BBSY
SACK
QBAR
CLRINT
INTR
ENA
7442



REVISIONS			
ZONE	LTR	DESCRIPTION	DATE / APPROVED
			7-26-79 DRS
			8/12/80 KPAU
			1/27/81 KAM

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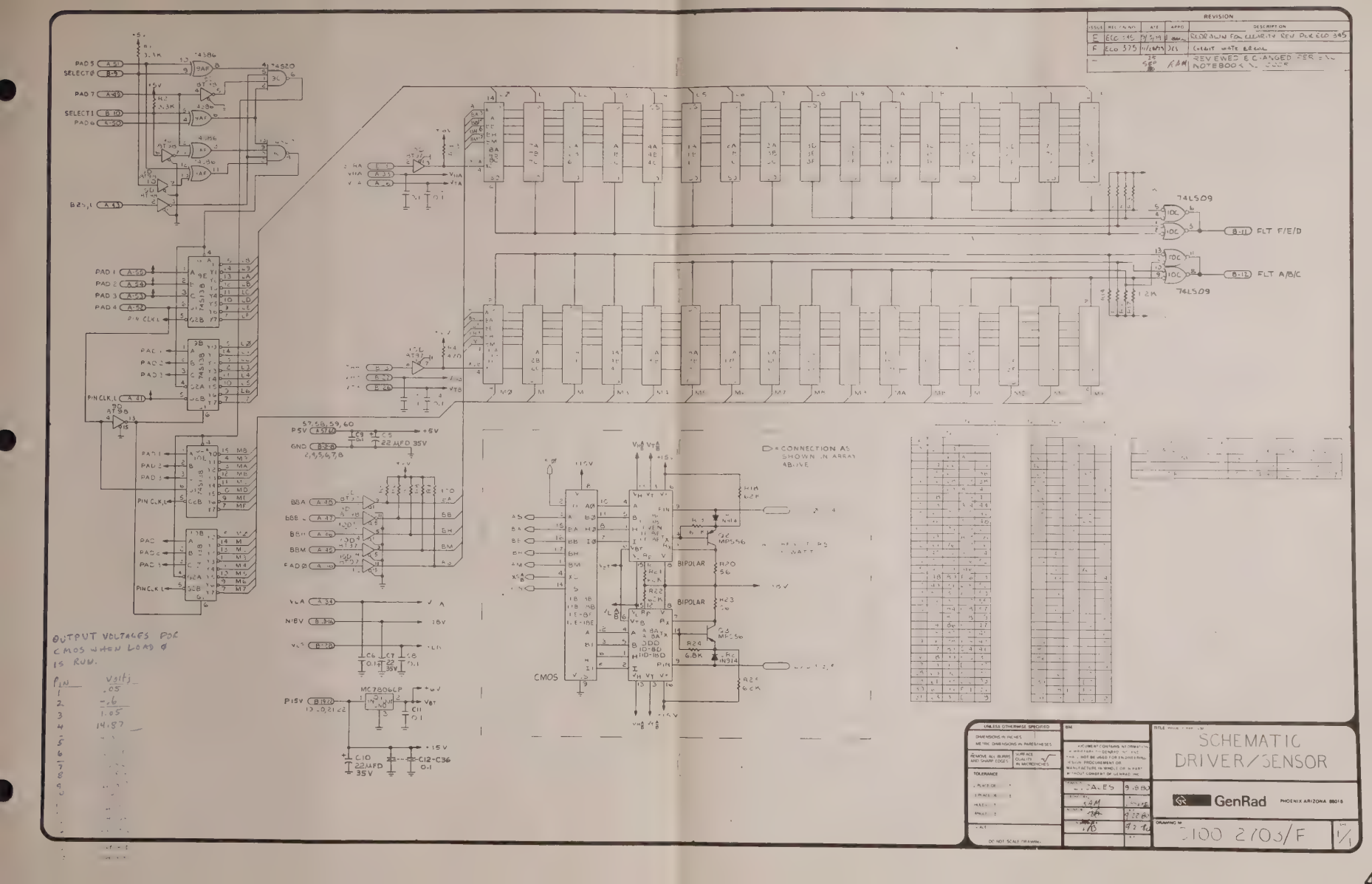
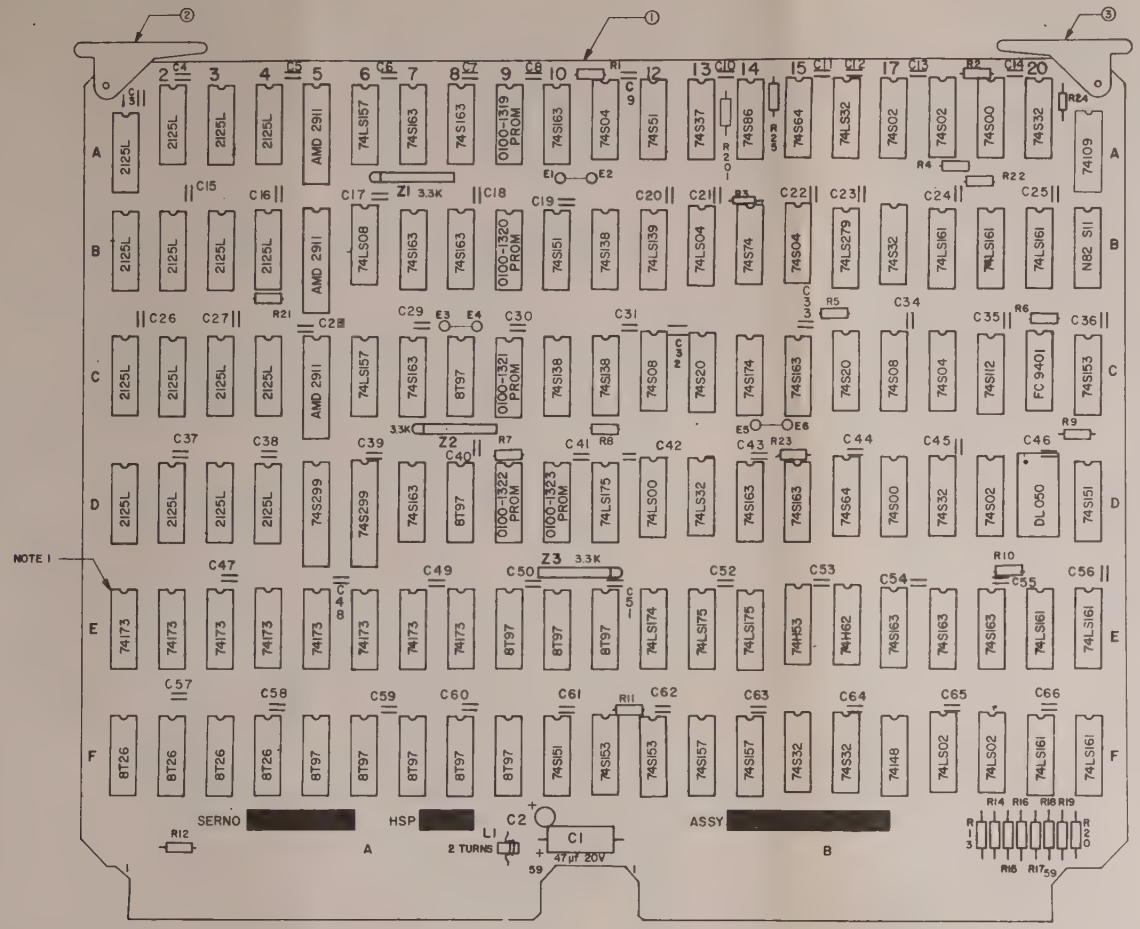
DRIVER SENSOR

SIZE	CODE IDENT NO	DRAWING NO	REV
D		0103-2703	F

SCALE | SHEET 1 OF


REVISION
DESCRIPTION
REDRAWN FOR CLARITY REV PER ECO 345
CHANGE WIRE BRAID
REVIEWED & CHANGED PER ECO NOTEBOOK
SCHEMATIC DRIVER/SENSOR
GenRad
PHOENIX ARIZONA 85015
74LS09
FLT F/E/D
FLT A/B/C
CMOS
BIPOLAR
OUTPUT VOLTAGES FOR CMOS WHEN LOAD # IS RUN.
PIN Volts
1 .05
2 -.6
3 1.05
4 14.87

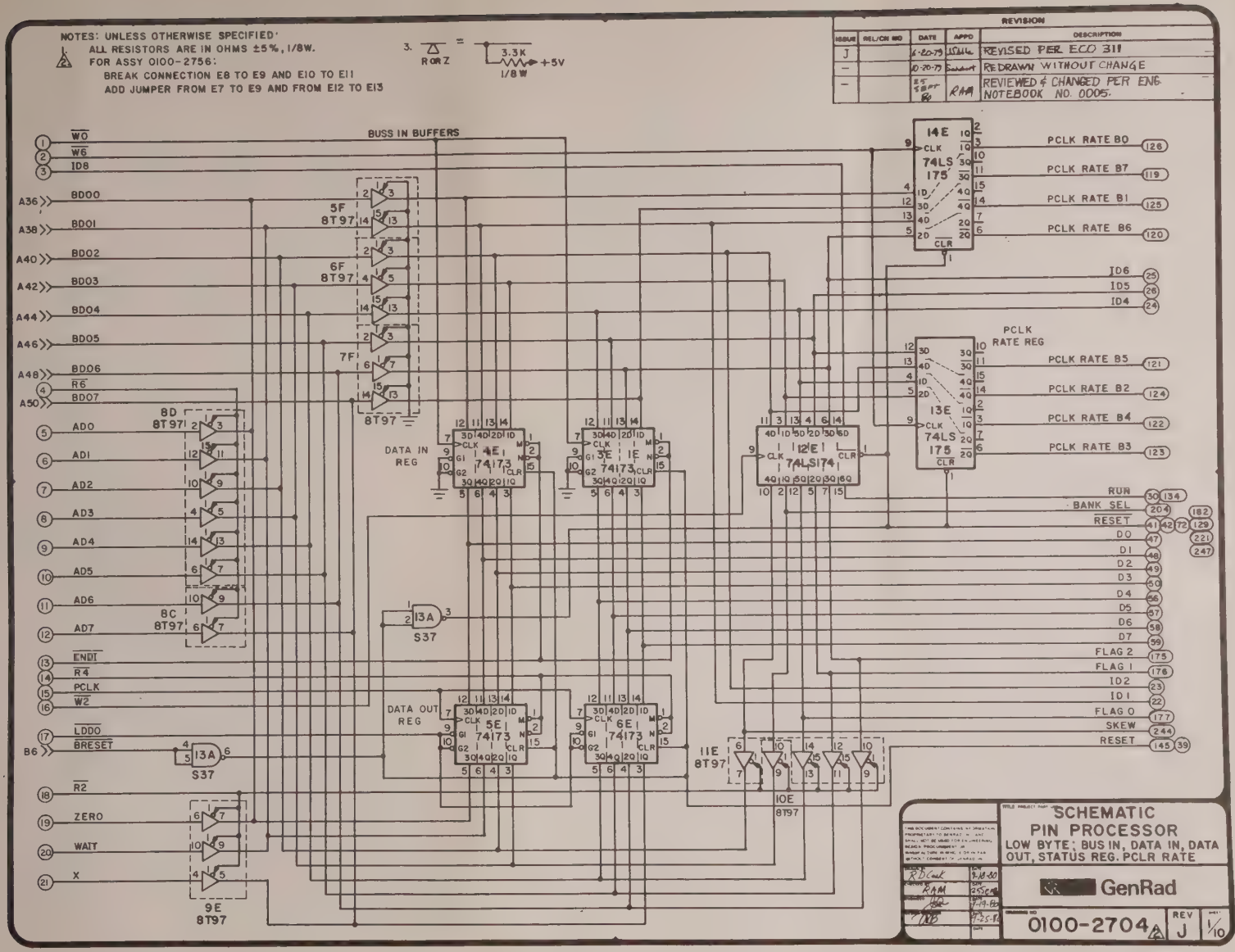


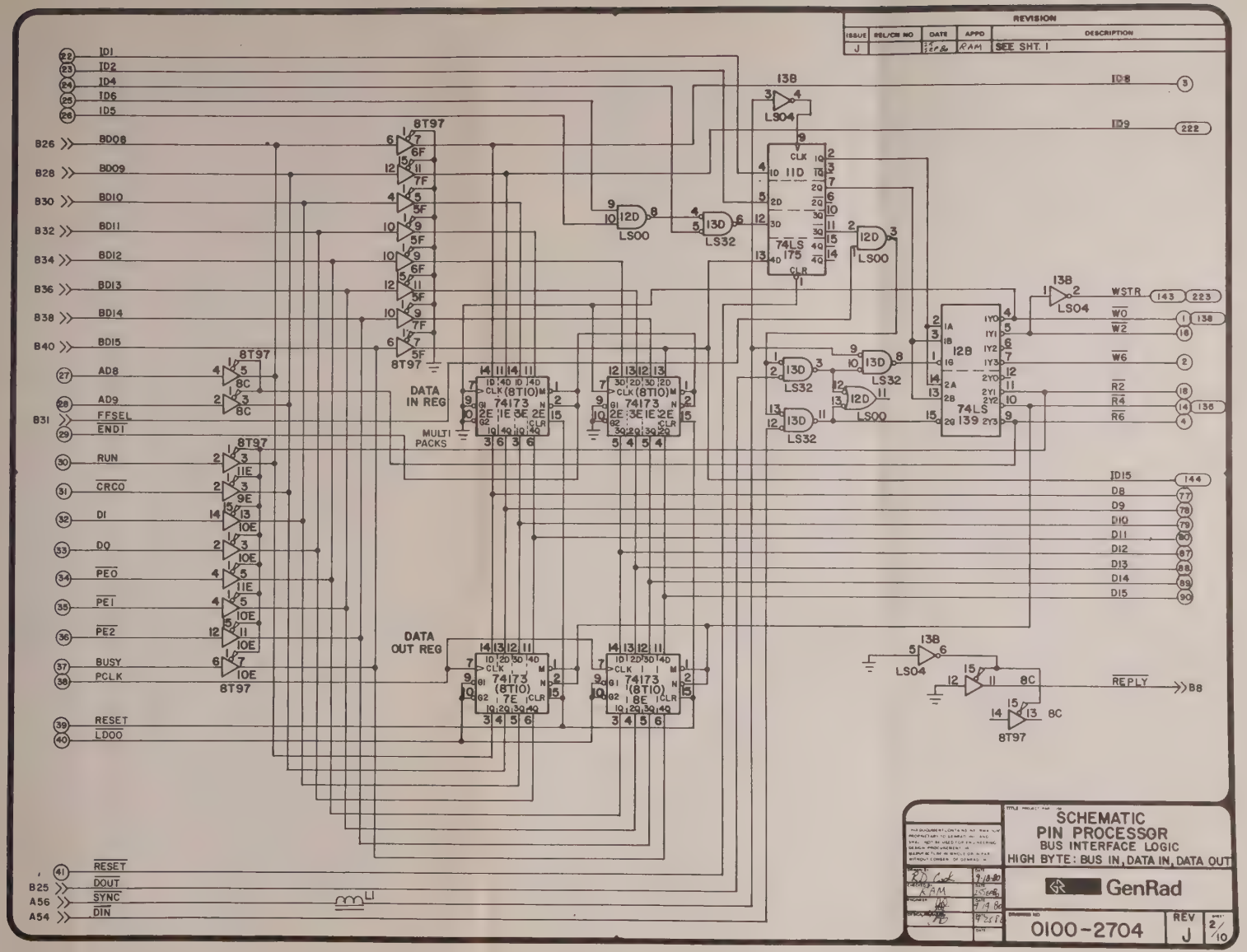
REVISION				
ISSUE	REL'S NO.	DATE	APPD	DESCRIPTION
K		6 7 79	LRT	REVISED PER ECO 311
M		12 2 79	DRS	REVISED PER ECO 371
J	9500-30	12 5 79	JLW	ORIGINATED ASSY DRWG
K		7 2 80	BRW	REV PER ECO 417
-		9-19-80	RAM	REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005

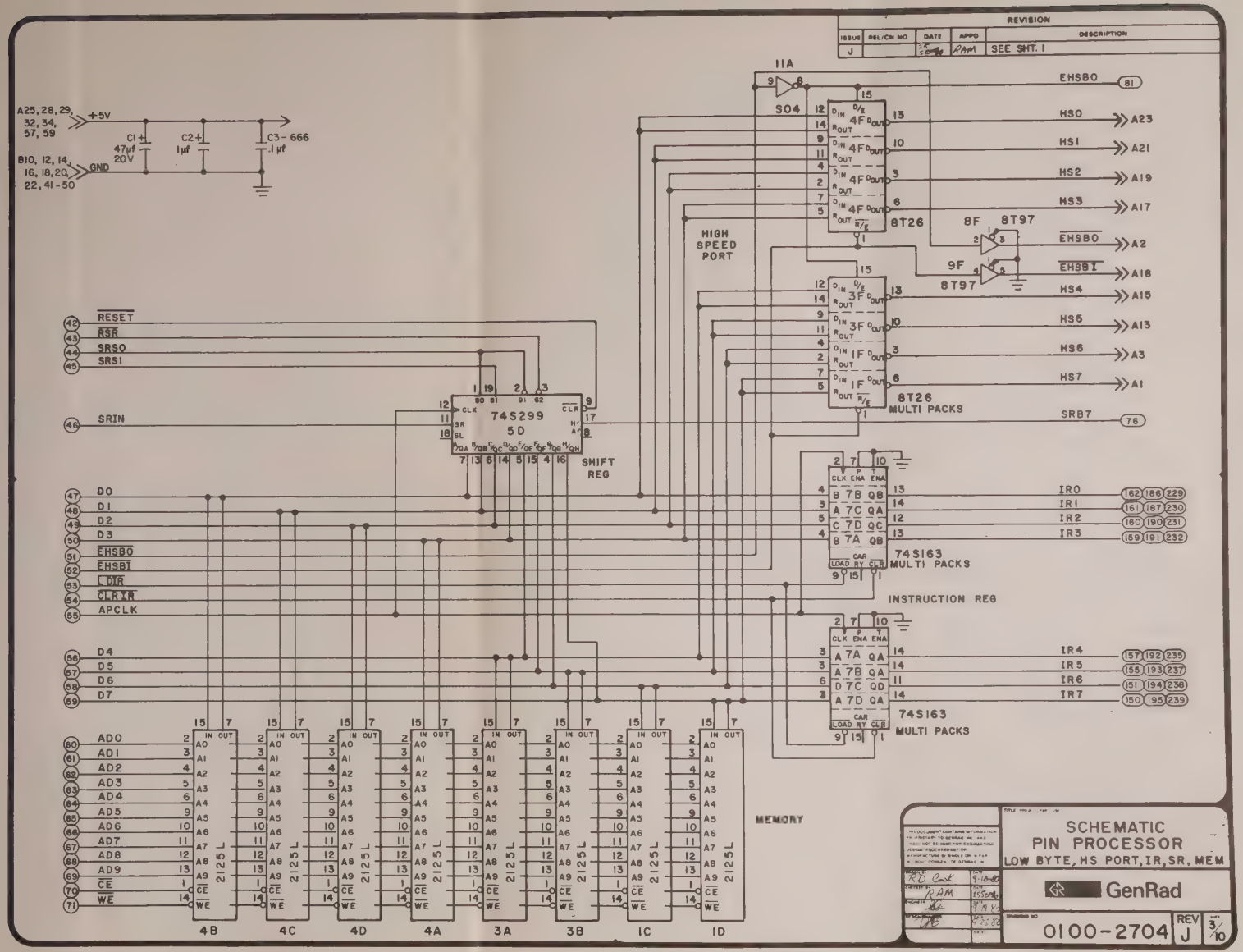
1. ALTERNATE IC TYPE FOR LOCATIONS 1E THRU 8E IS 8T10.

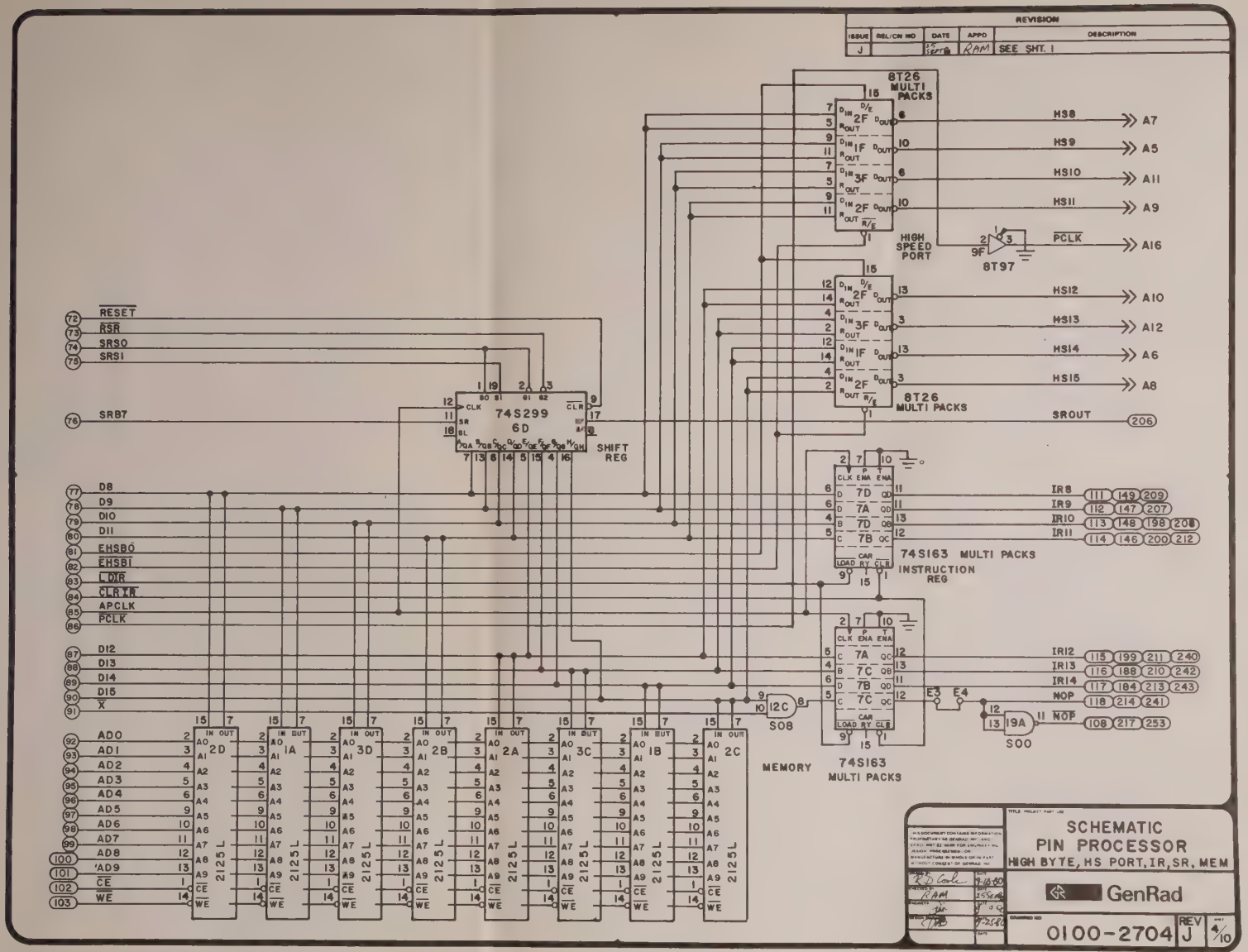
NOTES:

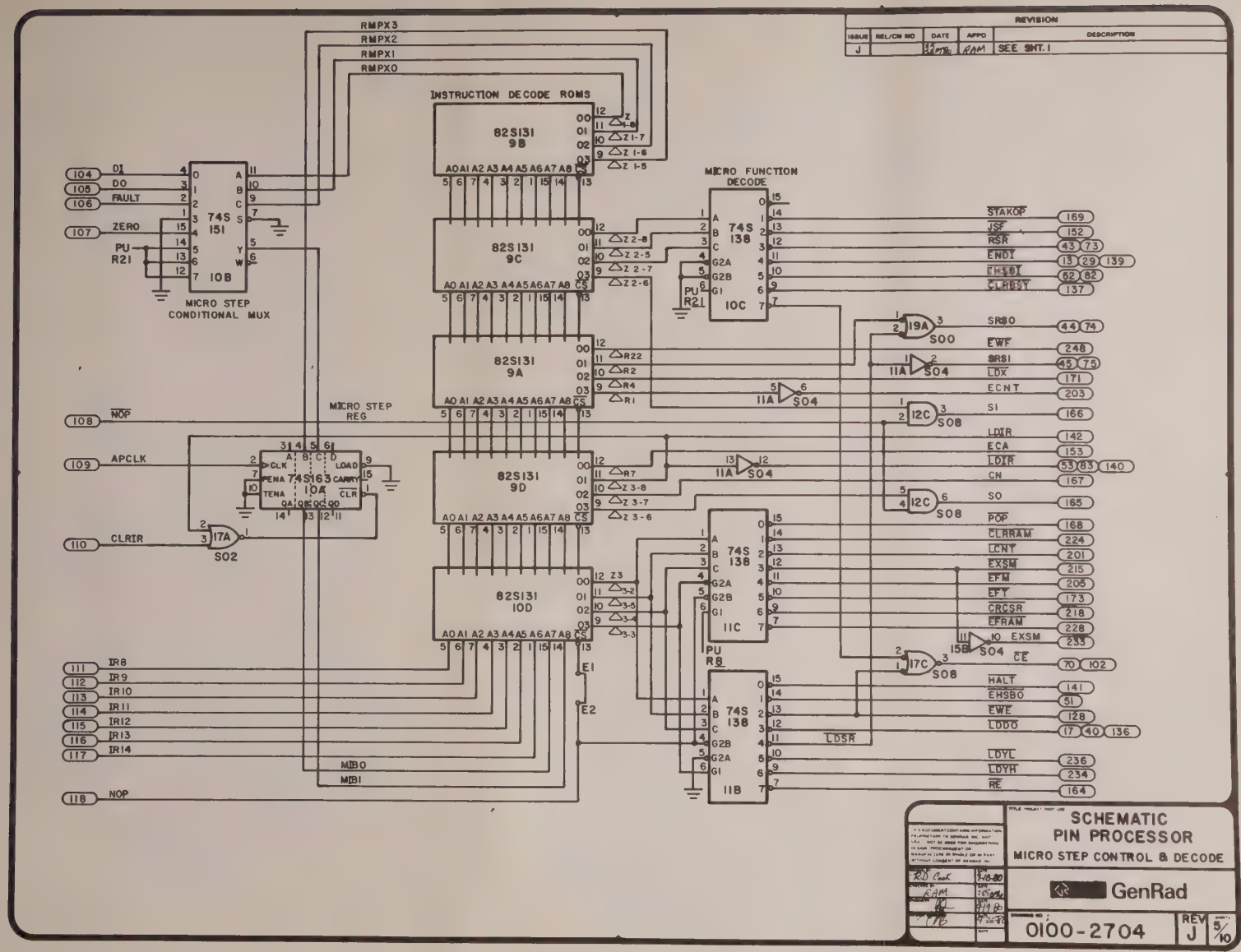
UNLESS OTHERWISE SPECIFIED		CIRCUIT CARD ASSEMBLY
DIMENSIONS IN INCHES		PSP PIN PROCESSOR BD
METRIC DIMENSIONS IN PARENTHESES		
REMOVE ALL BURRS AND SHARP EDGES	SURFACE FINISH 125 MICRO INCHES OR BETTER	GenRad PHOENIX ARIZONA 85016
TOLERANCE		
DRAWN	RD Cook 9-18-80	
CHECKED	RAM 9-19-80	
ENGR	9-19-80	
MFG	9-19-80	DRAWING NO 0100-2704/K
DO NOT SCALE DRAWING		SHEET 1/1

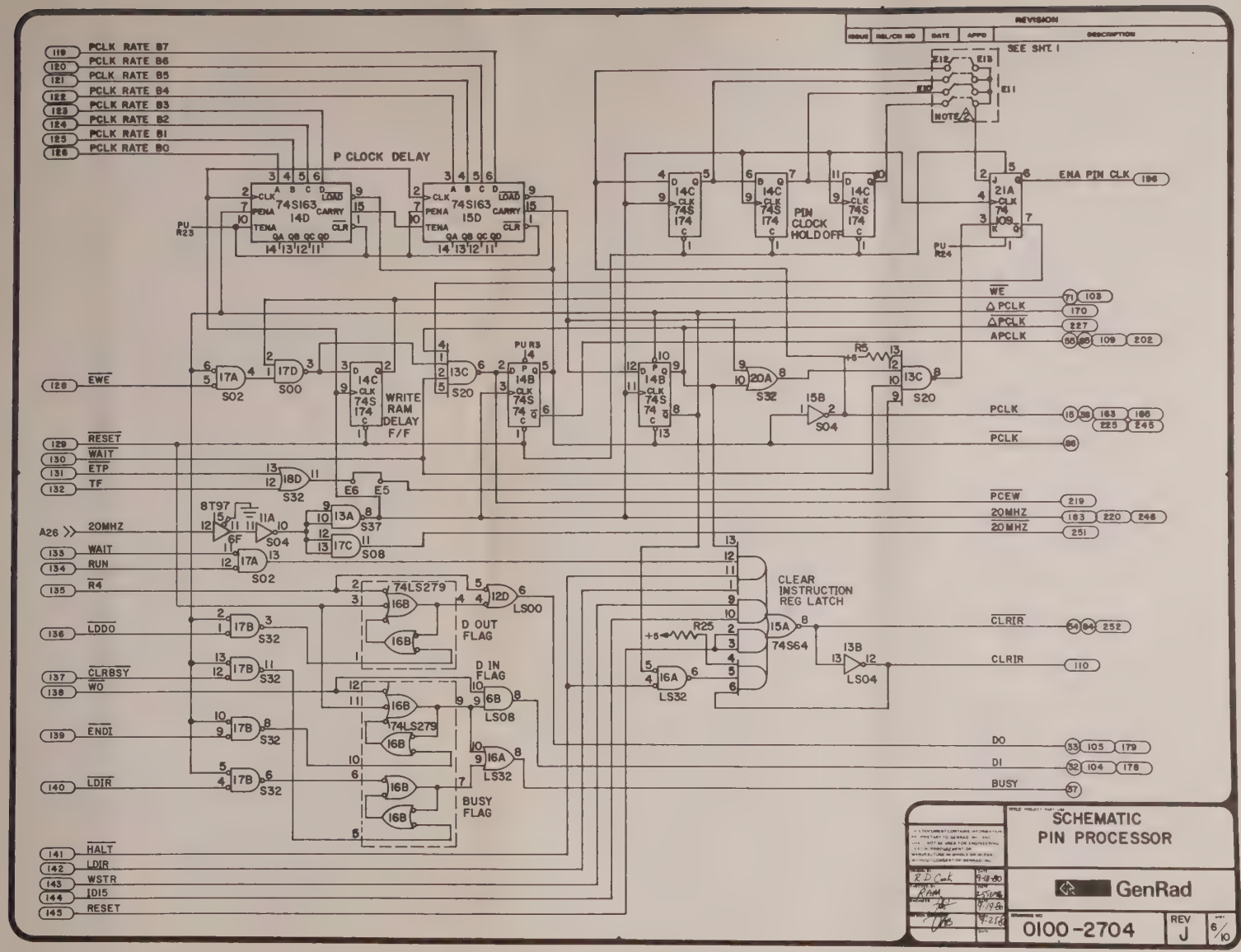

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS ±5%, 1/8W.
2. FOR ASSY 0100-2756:
BREAK CONNECTION E8 TO E9 AND E10 TO E11
ADD JUMPER FROM E7 TO E9 AND FROM E12 TO E13
3. R OR Z = 3.3K 1/8W +5V
REVISION
ISSUE REL/CN NO DATE APPD DESCRIPTION
J 4-20-79 REVISED PER ECO 311
– 10-20-79 REDRAWN WITHOUT CHANGE
– 25 OCT 80 RAM REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005.
BUSS IN BUFFERS
WO
W6
ID8
BD00
BD01
BD02
BD03
BD04
BD05
BD06
R6
BD07
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
ENDT
R4
PCLK
W2
LDDO
BRESET
R2
ZERO
WAIT
X
5F 8T97
6F 8T97
7F 8T97
8D 8T97
8C 8T97
9E 8T97
13A S37
DATA IN REG
4E 74173
3E 1E 74173
12E 74LS174
DATA OUT REG
5E 74173
6E 74173
11E 8T97
10E 8T97
14E 74LS 175
13E 74LS 175
PCLK RATE REG
PCLK RATE B0
PCLK RATE B7
PCLK RATE B1
PCLK RATE B6
PCLK RATE B5
PCLK RATE B2
PCLK RATE B4
PCLK RATE B3
ID6
ID5
ID4
RUN
BANK SEL
RESET
D0
D1
D2
D3
D4
D5
D6
D7
FLAG 2
FLAG 1
ID2
ID1
FLAG 0
SKEW
RESET
SCHEMATIC
PIN PROCESSOR
LOW BYTE; BUS IN, DATA IN, DATA OUT, STATUS REG. PCLR RATE
GenRad
0100-2704
REV J
SHEET 1/10

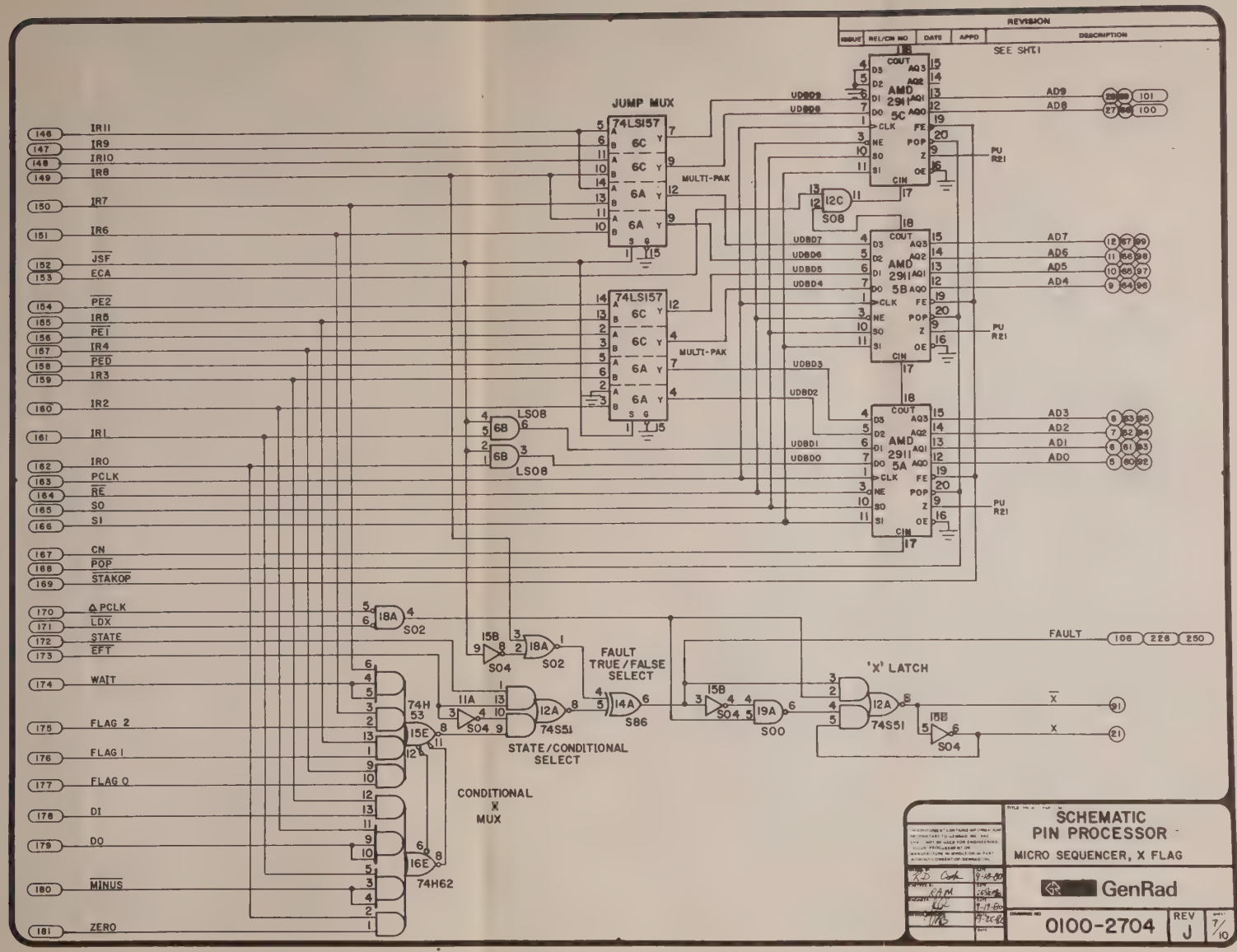

REVISION
ISSUE J
DESCRIPTION: SEE SHT. 1
SCHEMATIC
PIN PROCESSOR
BUS INTERFACE LOGIC
HIGH BYTE: BUS IN, DATA IN, DATA OUT
GenRad
0100-2704
REV J
DATA IN REG
DATA OUT REG
MULTI PACKS
ID1
ID2
ID4
ID6
ID5
BD08
BD09
BD10
BD11
BD12
BD13
BD14
BD15
AD8
AD9
FFSEL
ENDI
RUN
CRCO
DI
DO
PEO
PEI
PE2
BUSY
PCLK
RESET
LDOO
DOUT
SYNC
DIN
ID8
ID9
WSTR
W0
W2
W6
R2
R4
R6
ID15
D8
D9
D10
D11
D12
D13
D14
D15
REPLY
74173
74LS175
74LS139
LS00
LS04
LS32
8T97

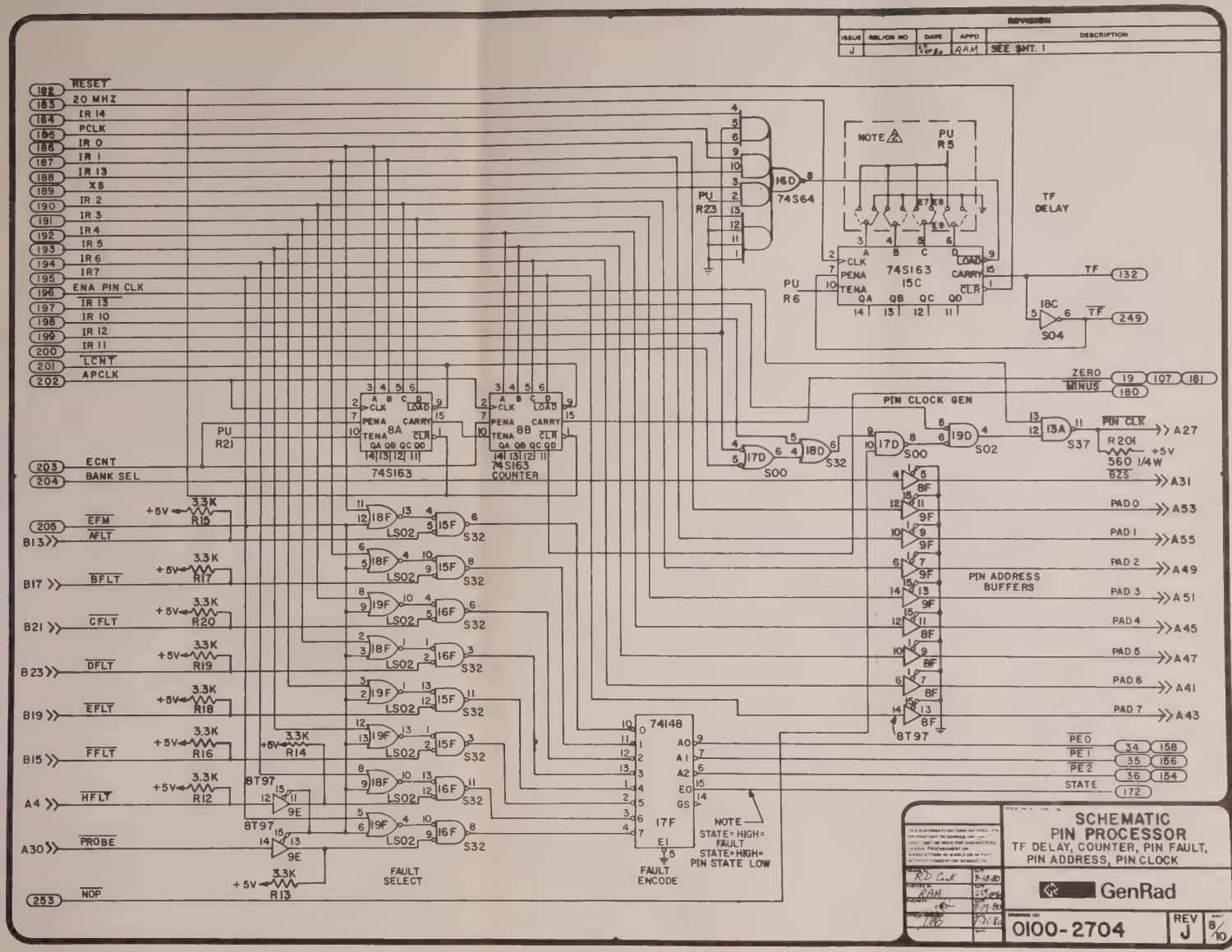

REVISION
ISSUE J
DESCRIPTION SEE SHT. 1
A25, 28, 29, 32, 34, 57, 59 +5V
B10, 12, 14, 16, 18, 20, 22, 41-50 GND
C1 47µf 20V
C2 1µf
C3-666 .1µf
11A
S04
EHSB0 (81)
HS0 A23
HS1 A21
HS2 A19
HS3 A17
8T26
HIGH SPEED PORT
8F 8T97
9F 8T97
EHSB0 A2
EHSB1 A18
HS4 A15
HS5 A13
HS6 A3
HS7 A1
8T26 MULTI PACKS
SRB7 (76)
RESET
RSR
SRS0
SRS1
SRIN
74S299 5D
SHIFT REG
D0
D1
D2
D3
EHSB0
EHSB1
L DIR
CLRIR
APCLK
D4
D5
D6
D7
IR0 (162) (186) (229)
IR1 (161) (187) (230)
IR2 (160) (190) (231)
IR3 (159) (191) (232)
74S163 MULTI PACKS
INSTRUCTION REG
IR4 (157) (192) (235)
IR5 (155) (193) (237)
IR6 (151) (194) (236)
IR7 (150) (195) (239)
74S163 MULTI PACKS
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
CE
WE
2125L
4B 4C 4D 4A 3A 3B 1C 1D
MEMORY
SCHEMATIC
PIN PROCESSOR
LOW BYTE, HS PORT, IR, SR, MEM
GenRad
0100-2704
REV J
3/10

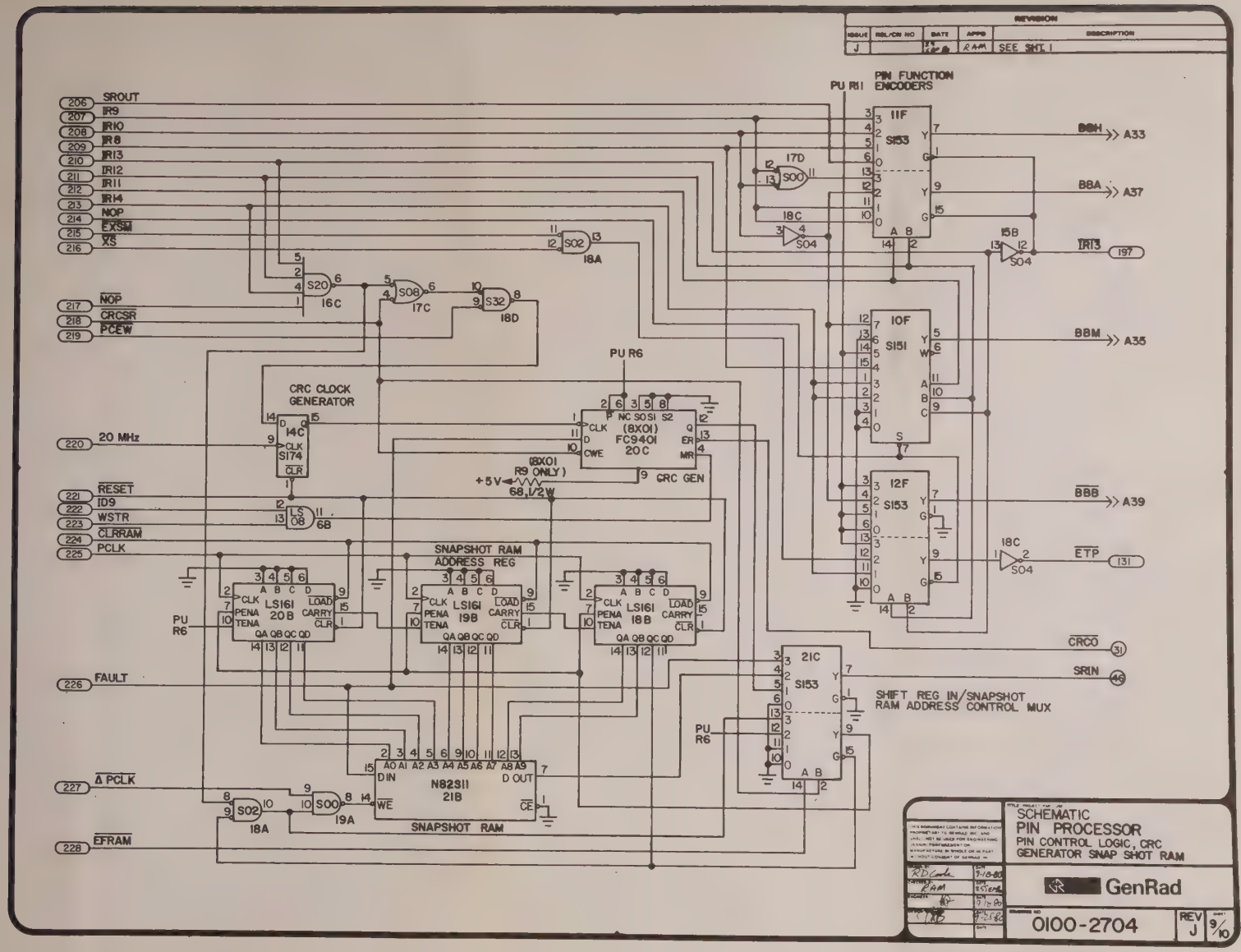

REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
J | | 25 SEPT 80 | RAM | SEE SHT. 1
8T26 MULTI PACKS
HIGH SPEED PORT
8T97
HS8
HS9
HS10
HS11
HS12
HS13
HS14
HS15
A7
A5
A11
A9
A16
A10
A12
A6
A8
PCLK
SROUT
206
RESET
RSR
SRSO
SRSI
SRB7
74S299
6D
SHIFT REG
D8
D9
DIO
DII
EHSBO
EHSBI
LDIR
CLRXR
APCLK
PCLK
D12
D13
D14
D15
X
74S163 MULTI PACKS
INSTRUCTION REG
IR8
IR9
IR10
IR11
IR12
IR13
IR14
NOP
NOP
S08
S00
MEMORY
74S163
MULTI PACKS
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
CE
WE
2125L
SCHEMATIC
PIN PROCESSOR
HIGH BYTE, HS PORT, IR, SR, MEM
GenRad
0100-2704
REV J
4/10

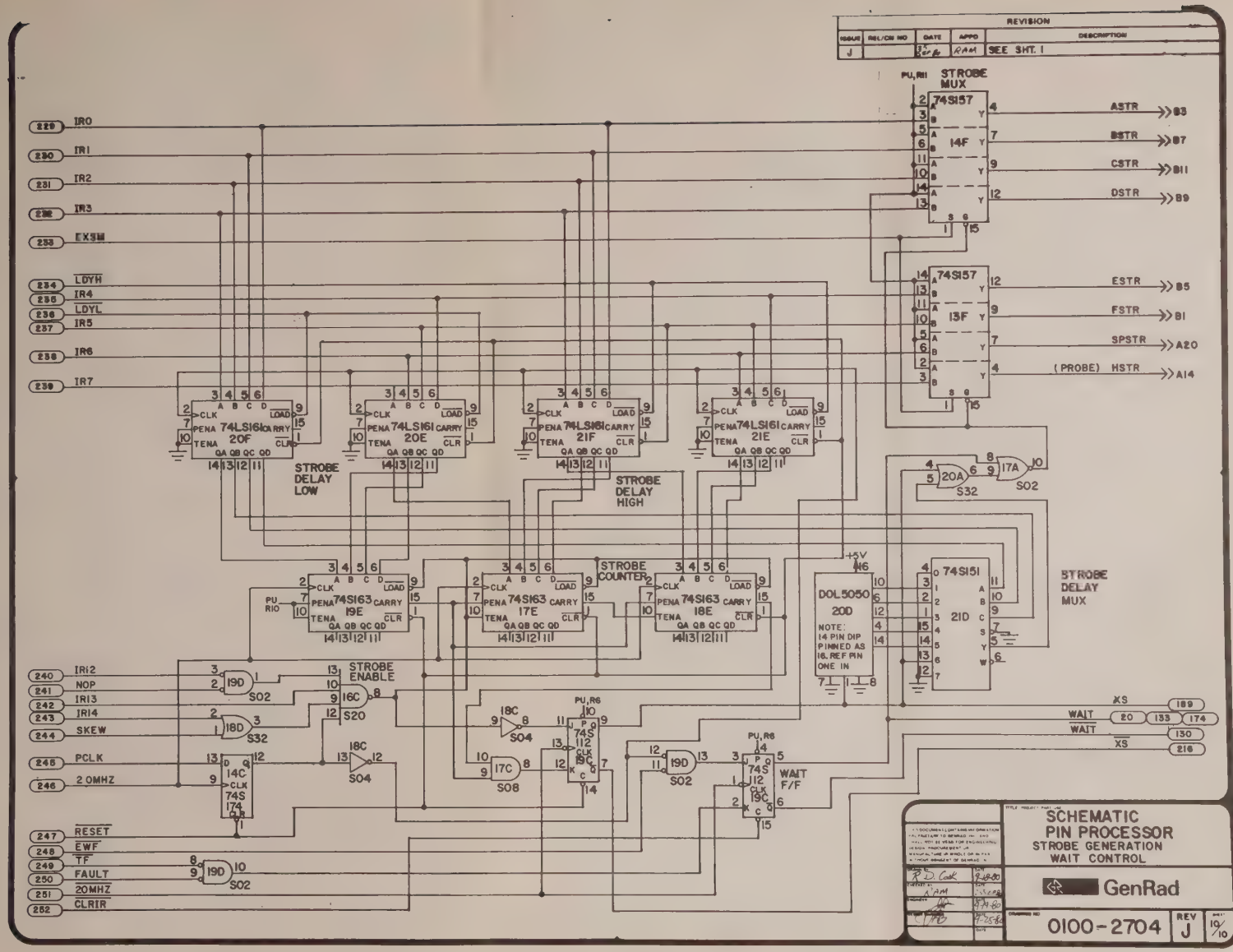

REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
J | | 12 MAR 80 | RAM | SEE SHT. 1
RMPX3
RMPX2
RMPX1
RMPX0
INSTRUCTION DECODE ROMS
82S131 9B
82S131 9C
82S131 9A
82S131 9D
82S131 10D
MICRO FUNCTION DECODE
74S 138 10C
74S 138 11C
74S 138 11B
74S 151 10B
MICRO STEP CONDITIONAL MUX
MICRO STEP REG
74S163 10A
104 DI
105 DO
106 FAULT
107 ZERO
PU R21
108 NOP
109 APCLK
110 CLRIR
111 IR8
112 IR9
113 IR10
114 IR11
115 IR12
116 IR13
117 IR14
118 NOP
MIBO
MIBI
E1
E2
STAKOP 169
JSF 152
RSR 43 73
ENDI 13 29 139
CLRBST 137
SRBO 44 74
EWF 248
SRBI 45 75
LDX 171
ECNT 203
SI 166
LDIR 142
ECA 153
LDDR 53 83 140
CN 167
SO 165
POP 168
CLRRAM 224
LCNT 201
EXSM 215
EFM 205
EFT 173
CRCSR 218
EFRAM 228
IO EXSM 233
CE 70 102
HALT 141
EMSBO 51
EWE 128
LDDO 17 40 136
LDSR
LDYL 236
LDYH 234
RE 164
SCHEMATIC
PIN PROCESSOR
MICRO STEP CONTROL & DECODE
GenRad
0100-2704
REV J
SHT 5/10


REVISION
SEE SHT 1
PCLK RATE B7
PCLK RATE B6
PCLK RATE B5
PCLK RATE B4
PCLK RATE B3
PCLK RATE B2
PCLK RATE B1
PCLK RATE B0
P CLOCK DELAY
74S163
14D
15D
PU R23
PU R24
PIN CLOCK HOLD OFF
ENA PIN CLK
WE
Δ PCLK
ΔPCLK
APCLK
EWE
WRITE RAM DELAY F/F
PU R3
R5
PCLK
PCEW
20MHZ
RESET
WAIT
ETP
TF
RUN
R4
LDDO
CLRBSY
WO
ENDI
LDIR
HALT
WSTR
ID15
CLEAR INSTRUCTION REG LATCH
R25
74S64
CLRIR
DO
DI
BUSY
74LS279
D OUT FLAG
D IN FLAG
BUSY FLAG
SCHEMATIC
PIN PROCESSOR
GenRad
0100-2704
REV J
6/10


REVISION
SEE SHT1
JUMP MUX
74LS157
MULTI-PAK
AMD 2911
IR11
IR9
IR10
IR8
IR7
IR6
JSF
ECA
PE2
IR5
PE1
IR4
PED
IR3
IR2
IR1
IR0
PCLK
RE
SO
SI
CN
POP
STAKOP
Δ PCLK
LDX
STATE
EFT
WAIT
FLAG 2
FLAG 1
FLAG 0
DI
DO
MINUS
ZERO
UDBD9
UDBD8
UDBD7
UDBD6
UDBD5
UDBD4
UDBD3
UDBD2
UDBD1
UDBD0
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PU
R21
LS08
S02
S04
S86
S00
74S51
74H53
74H62
FAULT
FAULT TRUE/FALSE SELECT
STATE/CONDITIONAL SELECT
CONDITIONAL X MUX
'X' LATCH
SCHEMATIC
PIN PROCESSOR
MICRO SEQUENCER, X FLAG
GenRad
0100-2704
REV J


REVISIONS
ISSUE J
DESCRIPTION SEE SHT. 1
182 RESET
183 20 MHZ
184 IR 14
185 PCLK
186 IR 0
187 IR 1
188 IR 13
189 XS
190 IR 2
191 IR 3
192 IR 4
193 IR 5
194 IR 6
195 IR 7
196 ENA PIN CLK
197 IR 13
198 IR 10
199 IR 12
200 IR 11
201 LCNT
202 APCLK
203 ECNT
204 BANK SEL
205 EFM
B13 AFLT
B17 BFLT
B21 CFLT
B23 DFLT
B19 EFLT
B15 FFLT
A4 HFLT
A30 PROBE
253 NOP
74S163
74S163 COUNTER
74S64
74S04
74S00
74S32
74S37
74148
74S163 15C
PU R21
PU R23
PU R6
PU R5
3.3K R15
3.3K R17
3.3K R20
3.3K R19
3.3K R18
3.3K R16
3.3K R14
3.3K R12
3.3K R13
560 1/4W R201
FAULT SELECT
FAULT ENCODE
NOTE STATE= HIGH= FAULT STATE= HIGH= PIN STATE LOW
TF DELAY
TF 132
TF 249
ZERO 19 107 181
MINUS 180
PIN CLOCK GEN
PIN CLK A27
BZS A31
PIN ADDRESS BUFFERS
PAD 0 A53
PAD 1 A55
PAD 2 A49
PAD 3 A51
PAD 4 A45
PAD 5 A47
PAD 6 A41
PAD 7 A43
PE0 34 158
PE1 35 156
PE2 36 154
STATE 172
SCHEMATIC
PIN PROCESSOR
TF DELAY, COUNTER, PIN FAULT, PIN ADDRESS, PIN CLOCK
GenRad
0100-2704
REV J
8/10


REVISION
ISSUE
REL/CN NO
DATE
APPD
DESCRIPTION
J
RAM
SEE SHT. 1
PIN FUNCTION ENCODERS
PU R11
SROUT
IR9
IR10
IR8
IR13
IR12
IR11
IR14
NOP
EXSM
XS
NOP
CRCSR
PCEW
20 MHz
RESET
ID9
WSTR
CLRRAM
PCLK
FAULT
Δ PCLK
EFRAM
CRC CLOCK GENERATOR
14C
S174
16C
17C
18D
18A
PU R6
20C
FC9401
(8X01)
(8X01 R9 ONLY)
+5V
68, 1/2W
CRC GEN
68
SNAPSHOT RAM ADDRESS REG
20B
19B
18B
LS161
PU R6
N82S11
21B
DIN
D OUT
WE
CE
SNAPSHOT RAM
19A
11F
10F
12F
21C
S153
17D
18C
15B
S04
S00
S02
S08
S32
S20
BBH
BBA
BBM
BBB
IRI3
ETP
CRCO
SRIN
A33
A37
A35
A39
197
131
31
45
SHIFT REG IN/SNAPSHOT RAM ADDRESS CONTROL MUX
SCHEMATIC
PIN PROCESSOR
PIN CONTROL LOGIC, CRC GENERATOR SNAP SHOT RAM
GenRad
0100-2704
REV J
9/10

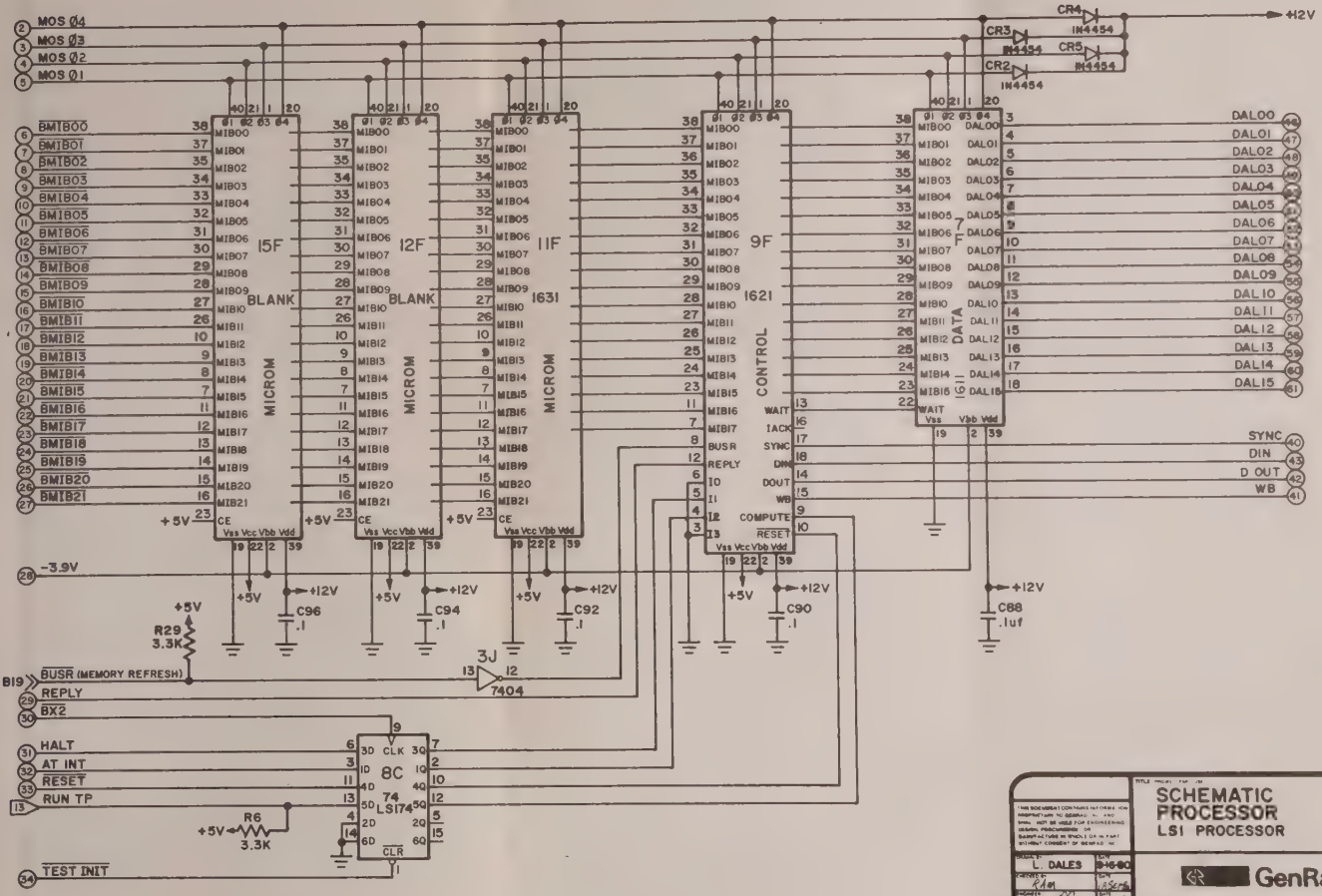

REVISION
ISSUE REL/CN NO DATE APPD DESCRIPTION
J RAM SEE SHT. 1
STROBE MUX
74S157 14F
ASTR B3
BSTR B7
CSTR B11
DSTR B9
74S157 13F
ESTR B5
FSTR B1
SPSTR A20
(PROBE) HSTR A14
IR0
IR1
IR2
IR3
EXSW
LDYH
IR4
LDYL
IR5
IR6
IR7
74LS161 20F
74LS161 20E
74LS161 21F
74LS161 21E
STROBE DELAY LOW
STROBE DELAY HIGH
20A S32
17A S02
74S163 19E
74S163 17E
74S163 18E
STROBE COUNTER
DOL5050 20D
NOTE: 14 PIN DIP PINNED AS 16. REF PIN ONE IN
74S151 21D
STROBE DELAY MUX
IR12
NOP
IR13
IR14
SKEW
19D S02
18D S32
STROBE ENABLE
16C S20
18C S04
17C S08
PCLK
2 0MHZ
14C 74S174
74S112 19C
WAIT F/F
RESET
EWF
TF
FAULT
20MHZ
CLRIR
XS
WAIT
WAIT
XS
SCHEMATIC
PIN PROCESSOR
STROBE GENERATION
WAIT CONTROL
GenRad
0100-2704
REV J

REV	DESCRIPTION	DATE	APPROVED
K	REL TO MFG NEW DRAWING 9500-31	12-13-79	JCS
	INC ECO 383	1-24-80	BRW
	REVIEWED & CHANGED PER ENG. NOTEBOOK NO.0005	9-16-80	RAM

		CIRCUIT CARD ASSY PROCESSOR BD	
		GenRad PHOENIX ARIZONA 85018	
		DRAWING NO 0100-2705	REV K 1/1

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTOR IN OHMS. ±5%, 1/4 W.
2. ALL CAPACITORS IN MICROFARADS.
3. ▷ = J1

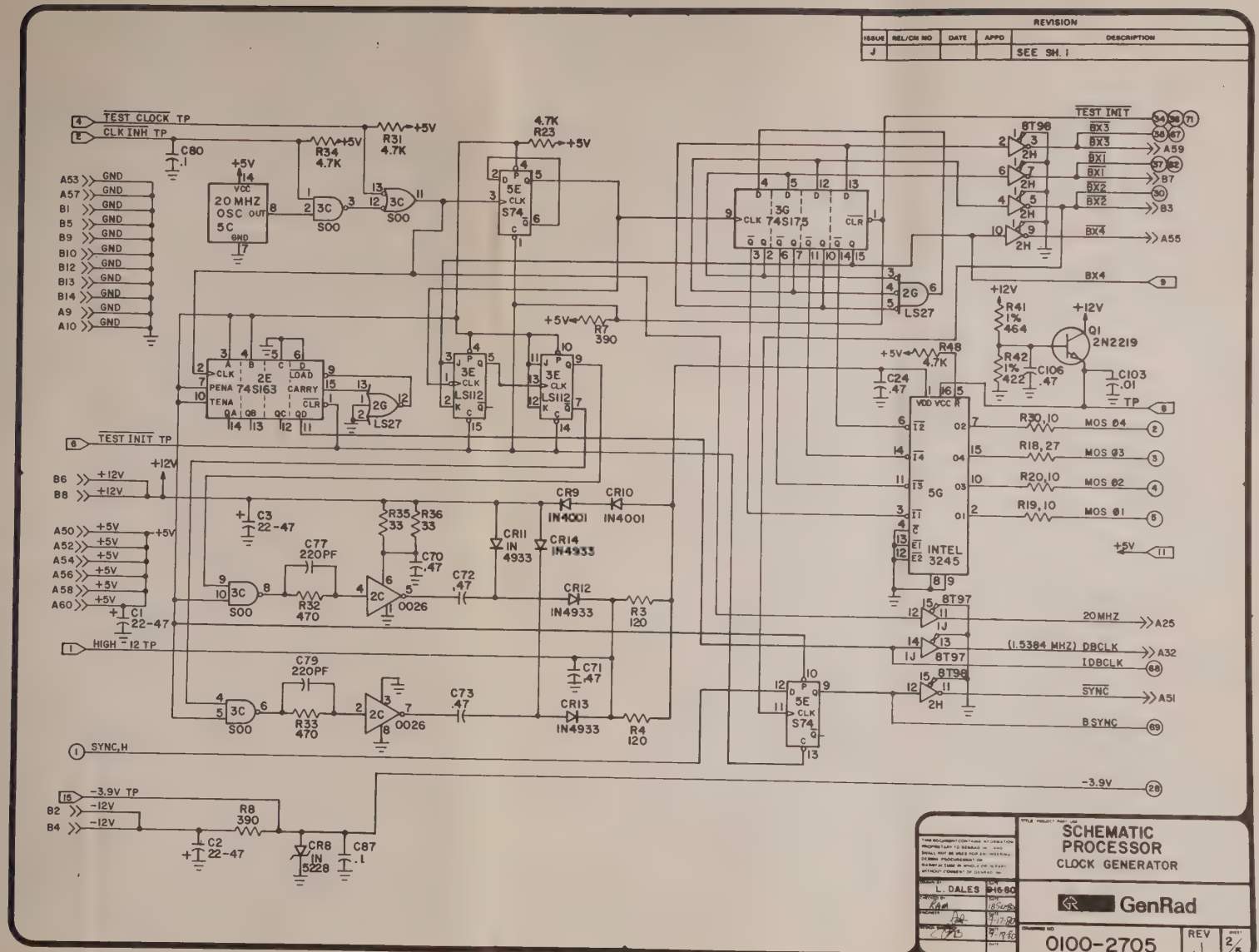
REVISION				
ISSUE	REL/CN NO	DATE	APPD	DESCRIPTION
H			JLW	REVISED PER E.C.O. 320
–		11-21-79		REDRAW WITHOUT CHANGE
J		7-22-80		REVISED PER ECO 389
J		18 Sep 80	RAM	REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005

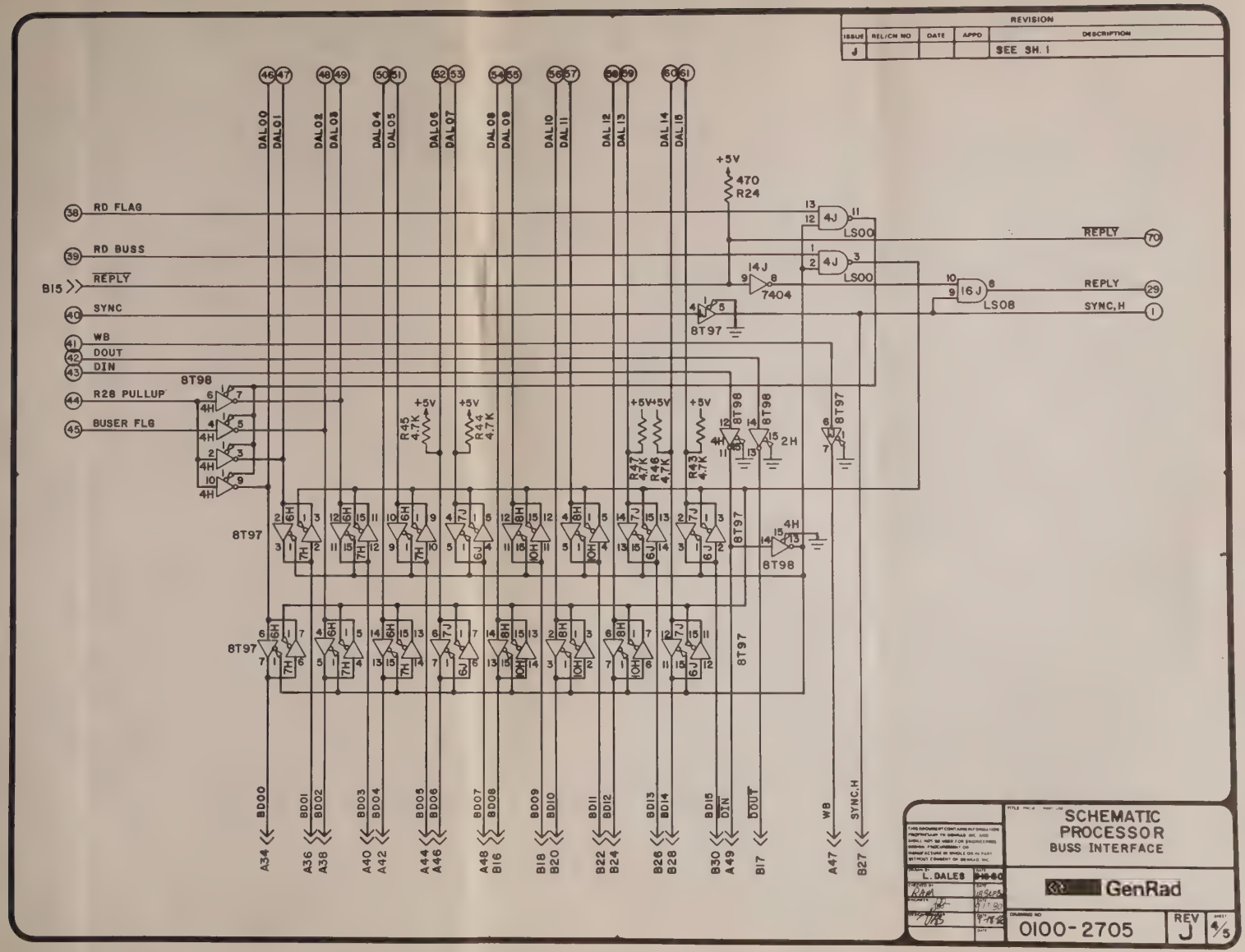


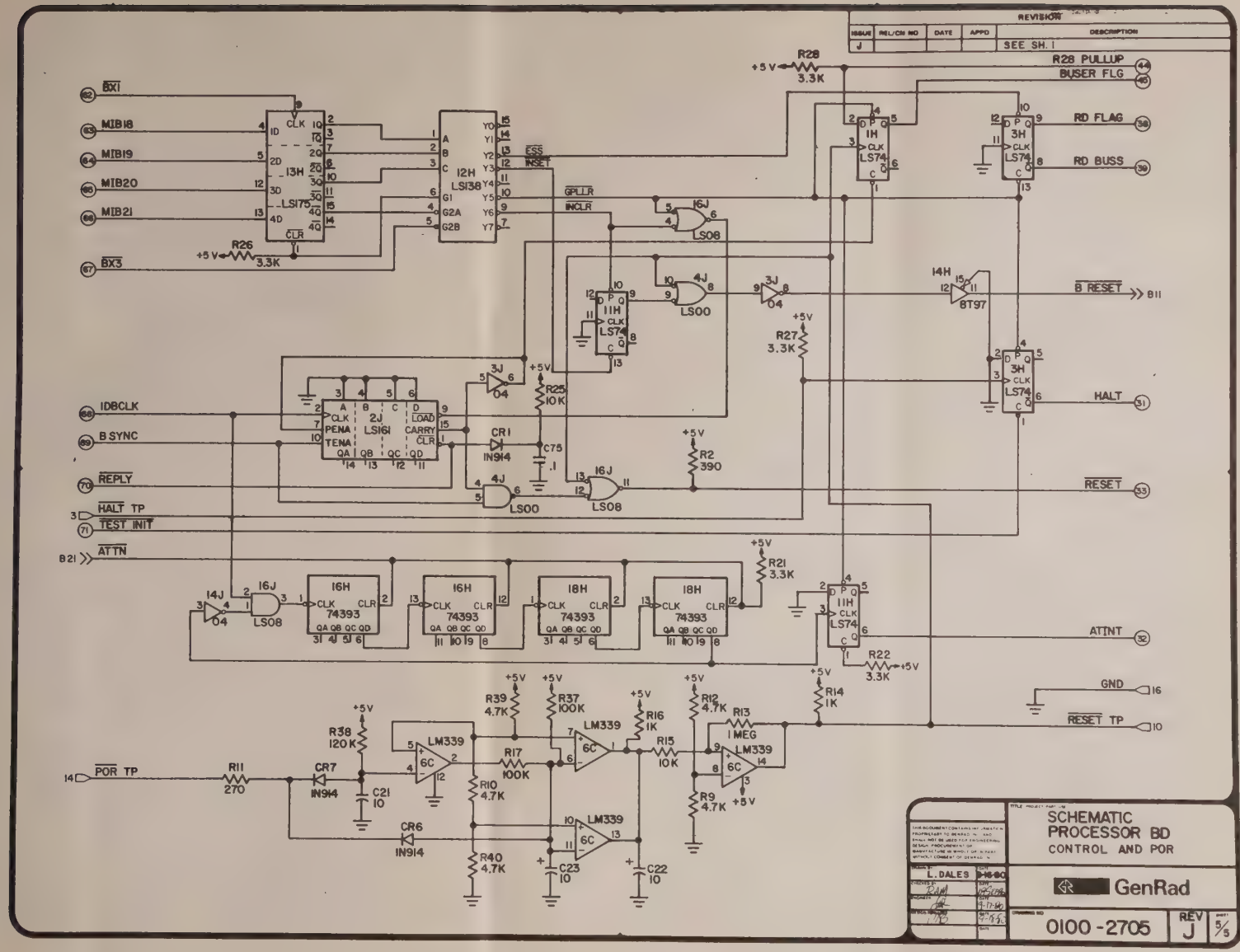
SCHEMATIC PROCESSOR
LSI PROCESSOR

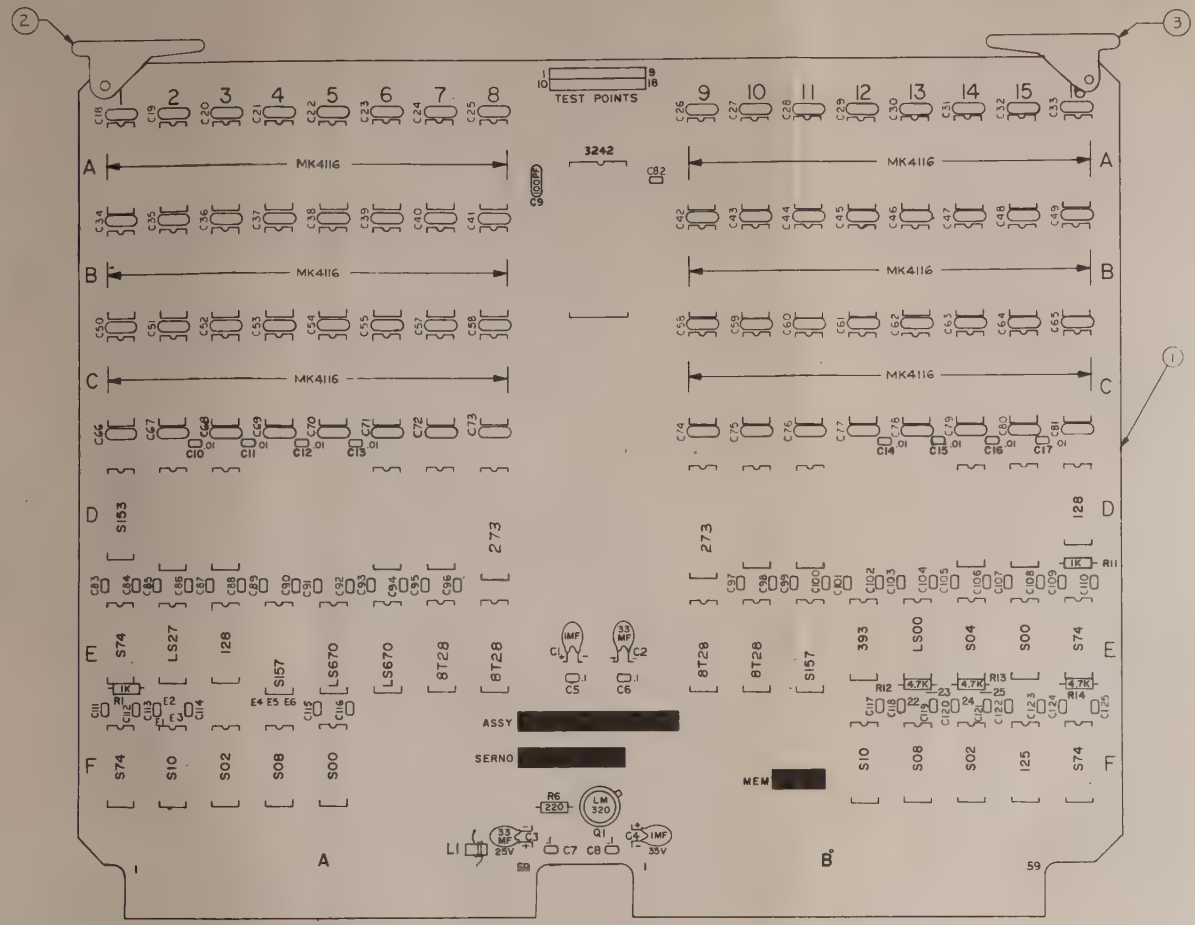
GenRad

0100-2705 REV J 1/5


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
J | | | | SEE SH. 1
TEST CLOCK TP
CLK INH TP
TEST INIT
TEST INIT TP
HIGH -12 TP
SYNC,H
-3.9V TP
20 MHZ OSC OUT 5C
74S163
LS27
LS112
74S175
74S74
INTEL 3245
8T98
8T97
IN4001
IN4933
2N2219
20MHZ
(1.5384 MHZ) DBCLK
IDBCLK
SYNC
BSYNC
SCHEMATIC PROCESSOR
CLOCK GENERATOR
L. DALES
GenRad
0100-2705
REV J
2/5


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
J | | | | SEE SH. 1
DAL00 DAL01 DAL02 DAL03 DAL04 DAL05 DAL06 DAL07 DAL08 DAL09 DAL10 DAL11 DAL12 DAL13 DAL14 DAL15
+5V
470 R24
RD FLAG
RD BUSS
REPLY
BI5
SYNC
WB
DOUT
DIN
R28 PULLUP
BUSER FLG
4J LS00
14J 7404
16J LS08
REPLY
SYNC,H
8T97
8T98
R45 4.7K
R44 4.7K
R47 4.7K
R46 4.7K
R43 4.7K
2H
4H
6H 7H
7J 6J
8H 10H
BD00 BD01 BD02 BD03 BD04 BD05 BD06 BD07 BD08 BD09 BD10 BD11 BD12 BD13 BD14 BD15
A34 A36 A38 A40 A42 A44 A46 A48 B16 B18 B20 B22 B24 B26 B28 B30 A49 B17 A47 B27
SCHEMATIC
PROCESSOR
BUSS INTERFACE
L. DALES
GenRad
0100-2705
REV J
1/5


REVISION
ISSUE J
SEE SH. 1
SCHEMATIC
PROCESSOR BD
CONTROL AND POR
GenRad
0100-2705
REV J
L. DALES
BX1
MIB18
MIB19
MIB20
MIB21
BX3
R26 3.3K
R28 3.3K
R28 PULLUP
BUSER FLG
RD FLAG
RD BUSS
B RESET
HALT
RESET
ATTNT
GND
RESET TP
IDBCLK
B SYNC
REPLY
HALT TP
TEST INIT
ATTN
B21
POR TP
R27 3.3K
R25 10K
R2 390
R21 3.3K
R22 3.3K
R14 1K
R11 270
R38 120K
R39 4.7K
R37 100K
R16 1K
R15 10K
R12 4.7K
R13 1MEG
R17 100K
R10 4.7K
R9 4.7K
R40 4.7K
CR1 IN914
CR7 IN914
CR6 IN914
C75 .1
C21 10
C23 10
C22 10
12H LSI38
13H LSI75
2J LSI61
16H 74393
18H 74393
LM339
LS00
LS08
LS74
8T97
04



REVISION			
REV	DESCRIPTION	DATE	
-	REVISED & REDRAWN SEE MARKED PRINT	1 27 78	
E1	REVISED PER ECO 1113	6-19 78	
F	REVISED PER ECO 242	3 30 79	
G	REVISED PER ECO 326	7-12-79	LRT
-	REDRAWN WITHOUT CHANGE PER ECO 337	7 7 79	JCS
H	REVISED PER ECO 355	10 11 79	JCS
J	REVISED PER ECO - 414	7 5 .	ERS
-	CHANGED PER ENG NOTEBOOK NC 0005	12 SEPT 80	RHM

1. MARK ASSY NO AND CURRENT REV. AT 37XX LEVEL.

NOTES (UNLESS OTHERWISE SPECIFIED)

		CIRCUIT CARD ASSEMBLY 96K MEMORY
DRAWN L. DALES	DATE 5-17-80	GenRad
CHECKED	DATE	
		DRAWING NO 0100-2722
SCALE		REV. J

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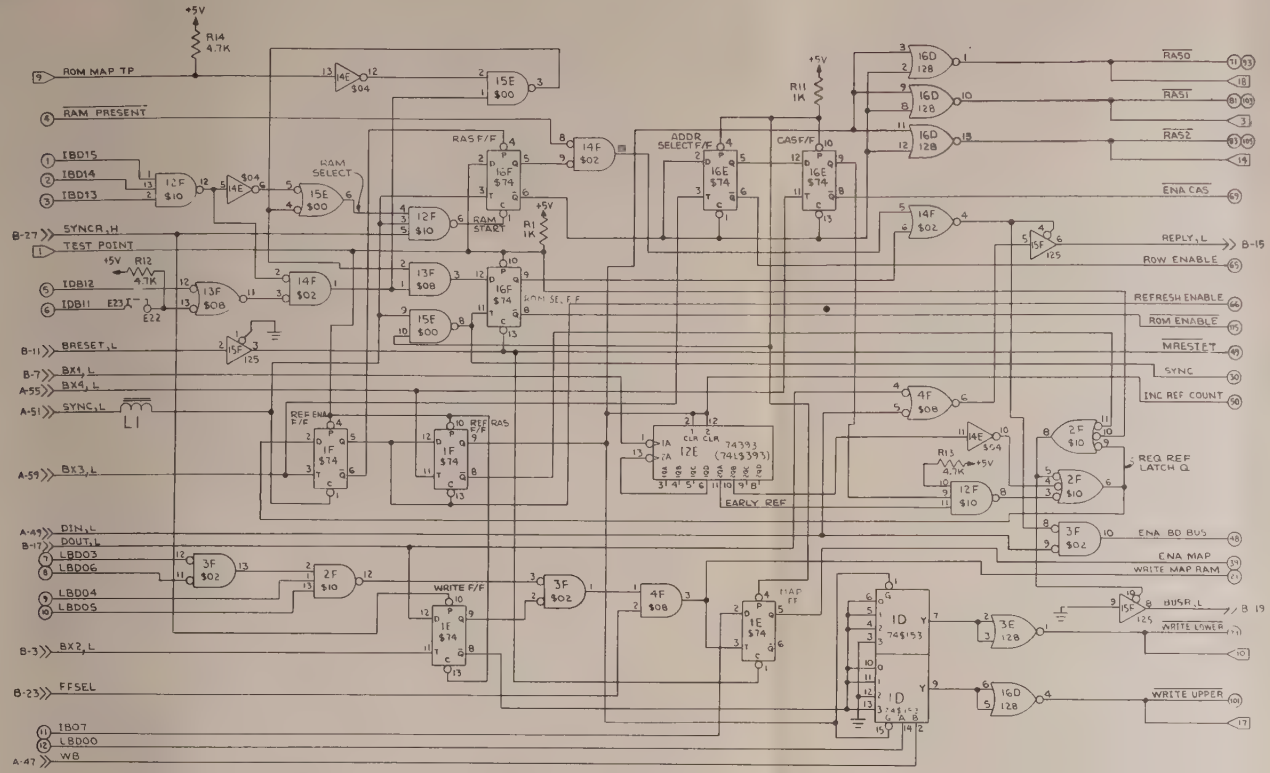
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	SCHEMATIC UPDATE PER MARKED PRINT	7-28-77	J. T
	B1	ADDED NOTE 1 TO FACE OF DWG JT	9 11	
	B2	ADDED CHOKE, REVISED U37,5 C 6 77		
	B3	REVISED NOTES.	11 8 77	
	D	UPDATED REV TO MATCH PACKAGE	12 78	
	E	UPDATED REV TO MATCH PACKAGE	1-26-78	JLW
	F	REVISED PER ECO 242	3-20 79	
	H	UPDATED PER ECO 355	11/9/79	JLS
	J	REVISED PER MARKED PRINT	8-27-80	J H
	—	REVIEWED & CHANGED PER ENG NOTEBOOK NO. 0005	26 SEPT 80	RAM



2. SYMBOLS:
» = EDGE CONNECTOR
▷ = TEST POINT

NOTES:

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DRAWN JS FROMM	9-17-80
CHECKED RAM	26 SEPT 80
ENGINEERING	9-23-80
APPROVED	9-25-80

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

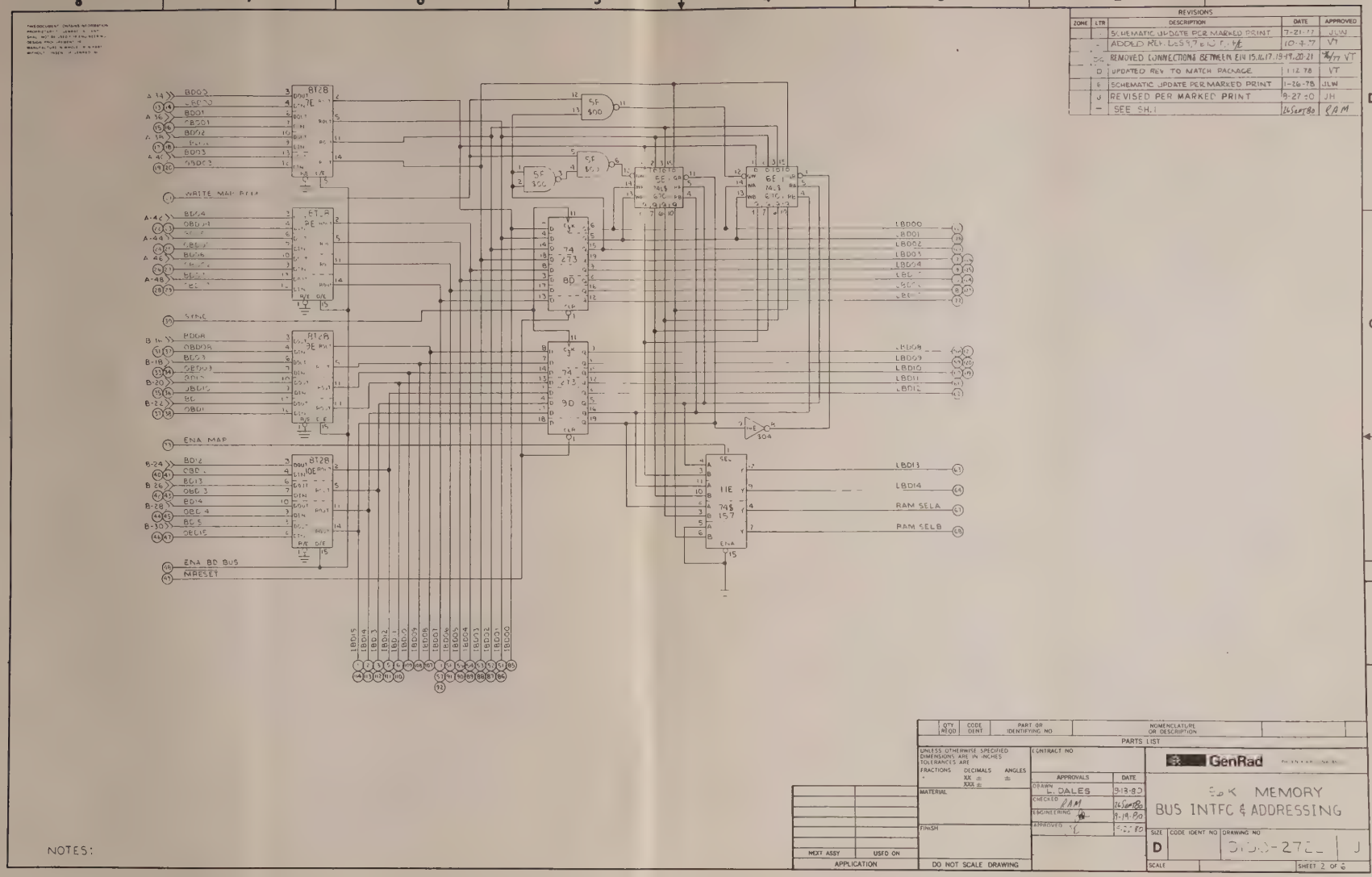
DO NOT SCALE DRAWING

GenRad PHOENIX ARIZONA 85016

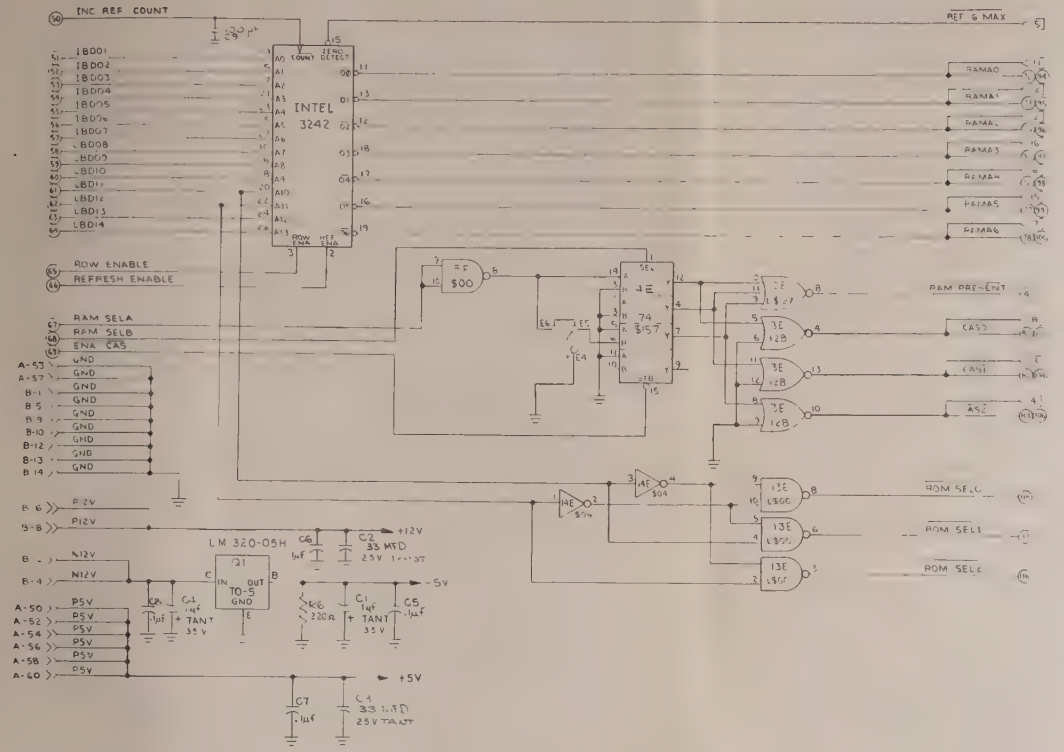
96K MEMORY CONTROL & TIMING

SIZE D | CODE IDENT NO. | DRAWING NO 0100-2722 J

SCALE | SHEET 1 OF 6


8
7
6
5
4
3
2
1
D
C
B
A
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
- | - | SCHEMATIC UPDATE PER MARKED PRINT | 7-21-77 | JLW
- | - | ADDED REV. LS377 & 'C' | 10-3-77 | VT
- | DC | REMOVED CONNECTIONS BETWEEN E14.15.16.17.18.19.20.21 | 3/4/77 | VT
- | D | UPDATED REV TO MATCH PACKAGE | 1-12-78 | VT
- | E | SCHEMATIC UPDATE PER MARKED PRINT | 1-26-78 | JLW
- | J | REVISED PER MARKED PRINT | 9-27-80 | JH
- | - | SEE SH.1 | 16SEPT80 | RAM
WRITE MAP PRM
ENA MAP
SYNC
ENA BD BUS
MRESET
LBD00
LBD01
LBD02
LBD03
LBD04
LBD08
LBD09
LBD10
LBD11
LBD12
LBD13
LBD14
RAM SELA
RAM SELB
NOTES:
PARTS LIST
QTY PER ASSY
CODE IDENT
PART OR IDENTIFYING NO
NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS
DECIMALS
XX ±
XXX ±
ANGLES
±
CONTRACT NO
APPROVALS
DATE
DRAWN L. DALES 9-3-80
CHECKED RAM 16SEP80
ENGINEERING 9-19-80
APPROVED 9-22-80
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
GenRad
64K MEMORY
BUS INTFC & ADDRESSING
SIZE D
CODE IDENT NO
DRAWING NO 0103-2721 J
SCALE
SHEET 2 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	SCHEMATIC UPDATE PER MARKED PRINT	7-21-77	JLWJ
	D	NEW UPDATED TO MATCH PACKAGE	1-12-78	VT
	E	SCHEMATIC UPDATE PER MARKED PRINT	1-26-78	JLW
	J	SCHEMATIC UPDATE PER MARKED PRINT	8-27-80	J H
	—	SEE SHEET 1	24SEPT80	RAM



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO

APPROVALS	DATE
DRAWN JS FROMM	9-17-80
CHECKED RAM	24SEPT80
ENGINEER	9-27-80
APPROVED	9-27-80

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

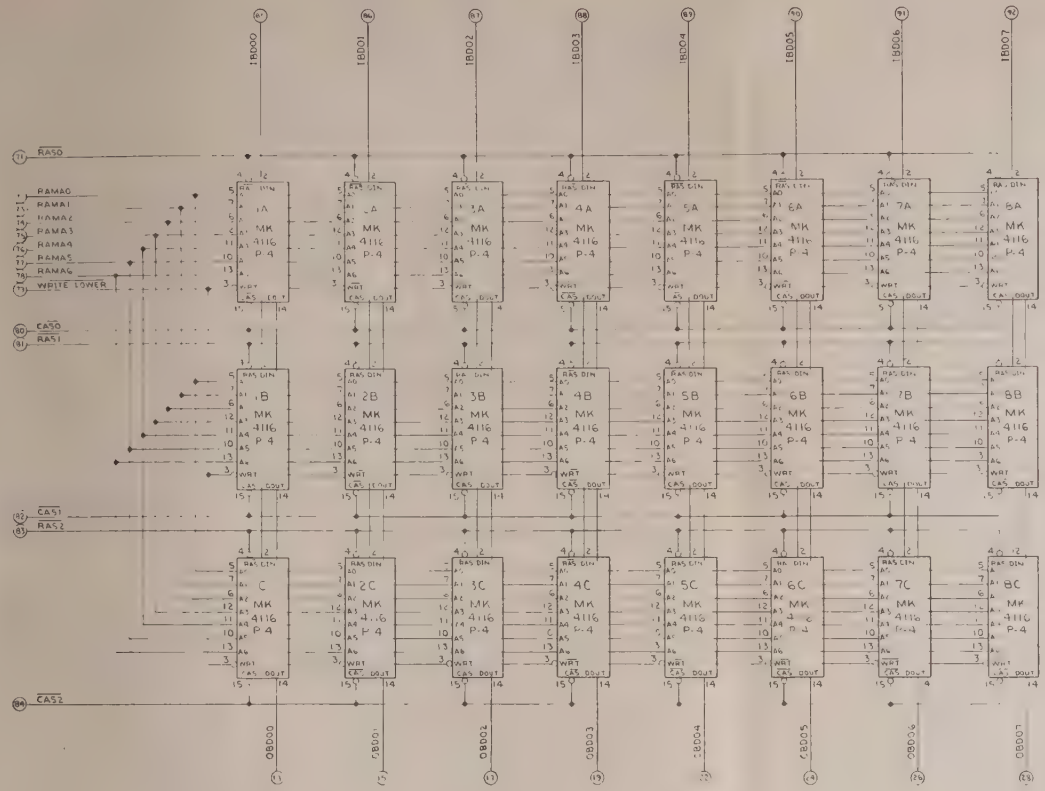
GenRad

96K MEMORY
REFRESH CONTROLLER

SIZE	CODE IDENT NO	DRAWING NO	
D		0100-2722	J

SCALE | SHEET 3 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	BY
	A	SCHEMATIC UPDATE PER MARKED PRINT	7-21-77	JLW
	D	REV UPDATED TO MATCH PACKAGE	1-12-78	VJT
	E	REV UPDATED TO MATCH PACKAGE	1-26-78	JLW
	J	SEE SHEET 1	26 OCT 80	RAM



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN JS FROMM	9-17-80
CHECKED RAM	26 OCT 80
ENG MGR'N	9 OCT 80
APPROVED	10 OCT 80

GenRad

32K MEMORY
LOW BYTE RAM

SIZE	CODE IDENT NO	DRAWING NO	
D		0100-2722	J

SCALE | SHEET 4 OF 6

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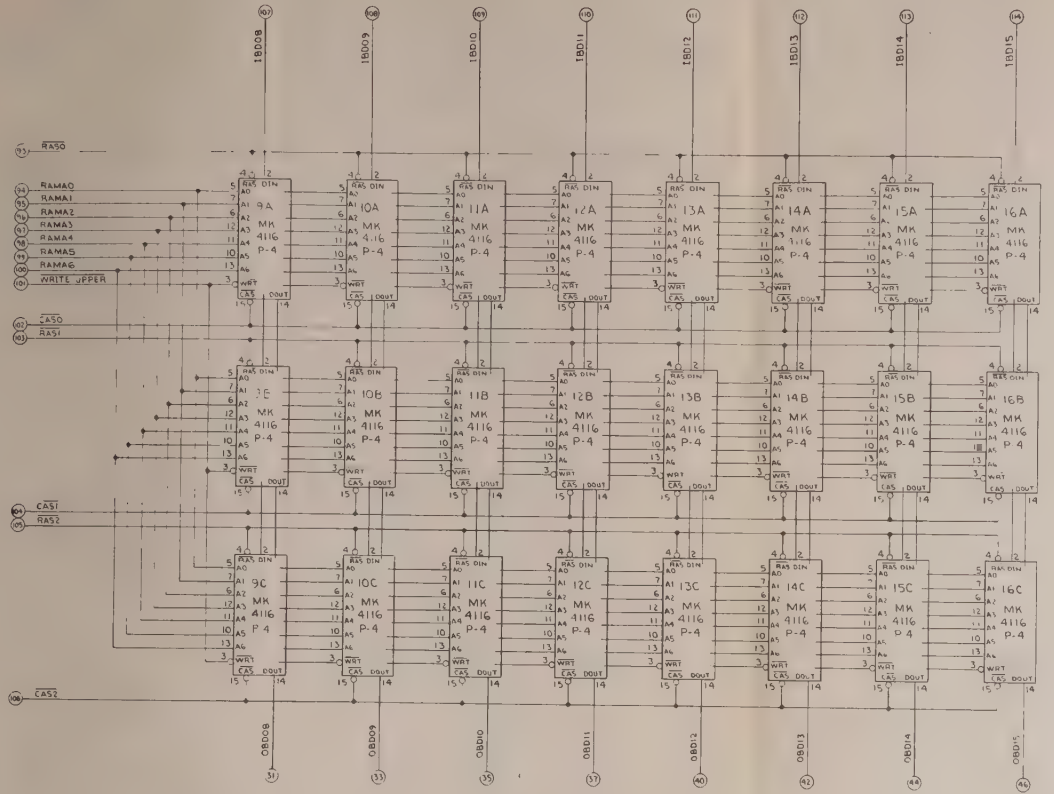
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	SCHEMATIC UPDATE PER MARKED PRINT	7-2-77	J.W
	D	REV. UPDATED TO MATCH PACKAGE	1-12-78	RJT
	E	REV UPDATED TO MATCH PACKAGE	1-26-78	J.W
	J	SEE SHT 1	24 APR 80	RAM



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN JS FROMM	3.79
CHECKED RAM	24 APR 80
ENGINEERING	4.7.80
APPR MFG	4.7.80

GenRad PHOENIX ARIZONA 85016

96K MEMORY
HIGH BYTE RAM

SIZE	CODE IDENT NO	DRAWING NO	
D		0100-27_	J

SCALE | SHEET 5 OF 6

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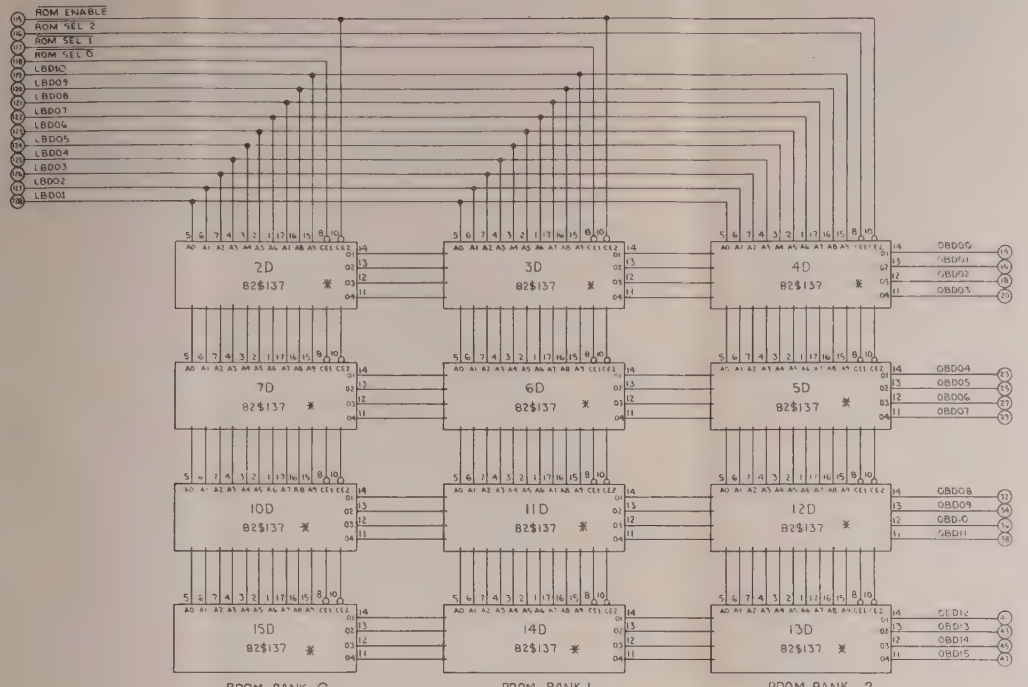
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	SCHEMATIC UPDATE PER MARKED PRINT	7-28-77	[illegible]
	D	REV UPDATE TO MATCH PACKAGE	12-7-78	VT
	E	REV UPDATED TO MATCH PACKAGE	1-26-78	JLW
	J	ADDED NOTE PER MARKED PRINT	8-27-80	JM
	—	SEE SHEET 1	12/8/77	RAM



* THE COMPONENTS REPRESENTED ON THIS SHEET ARE NOT PART OF THE 0100-2722 CIRCUIT BOARD ASSY. THEY ARE SHOWN HERE FOR REFERENCE ONLY.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN [illegible]	9-17-80
CHECKED RAM	12/8/77
ENGINEER [illegible]	9-23-80
APPROVED [illegible]	9-24-80

GenRad

9.5 K MEMORY
ROM

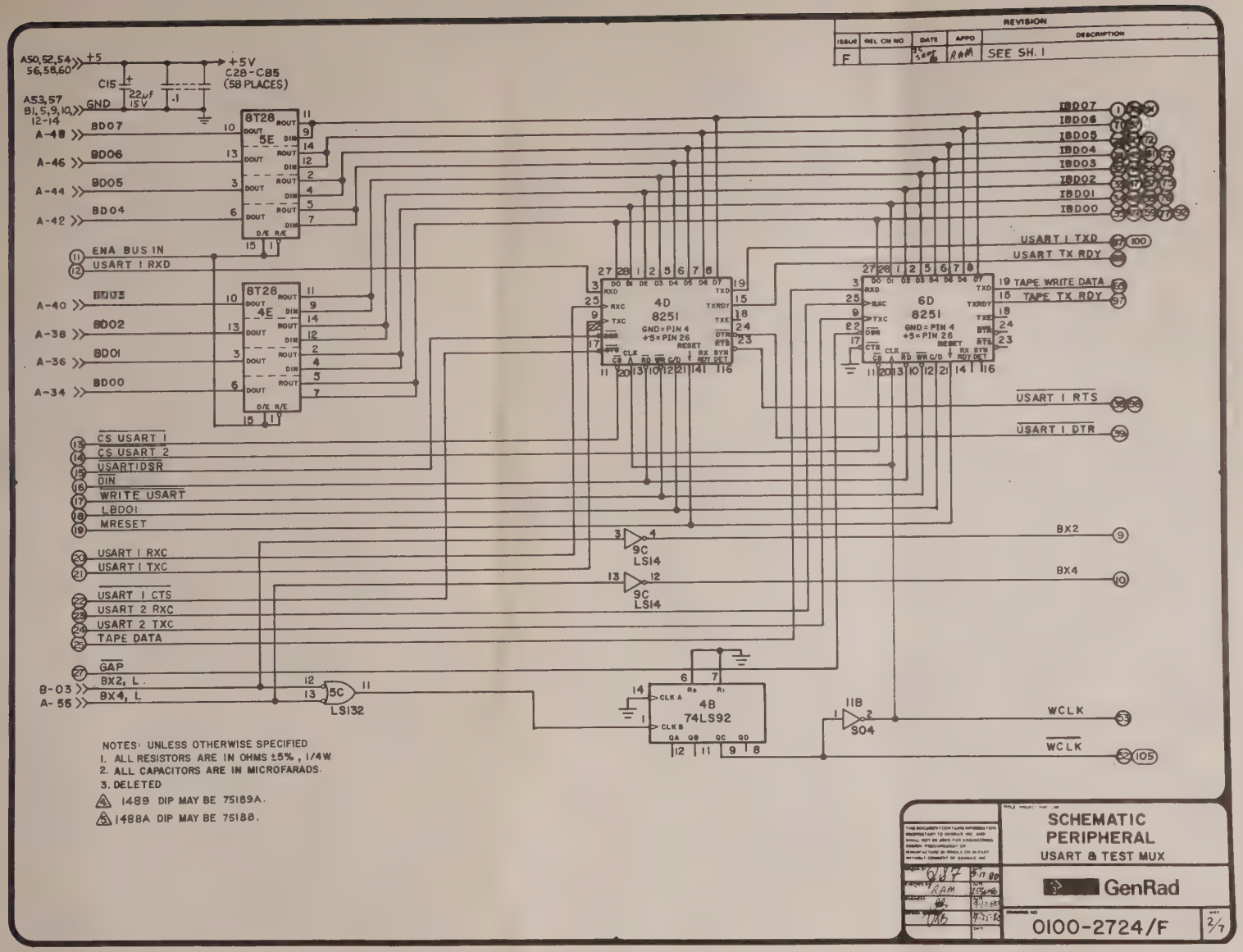
SIZE	CODE IDENT NO	DRAWING NO	
D		0100-2722	J

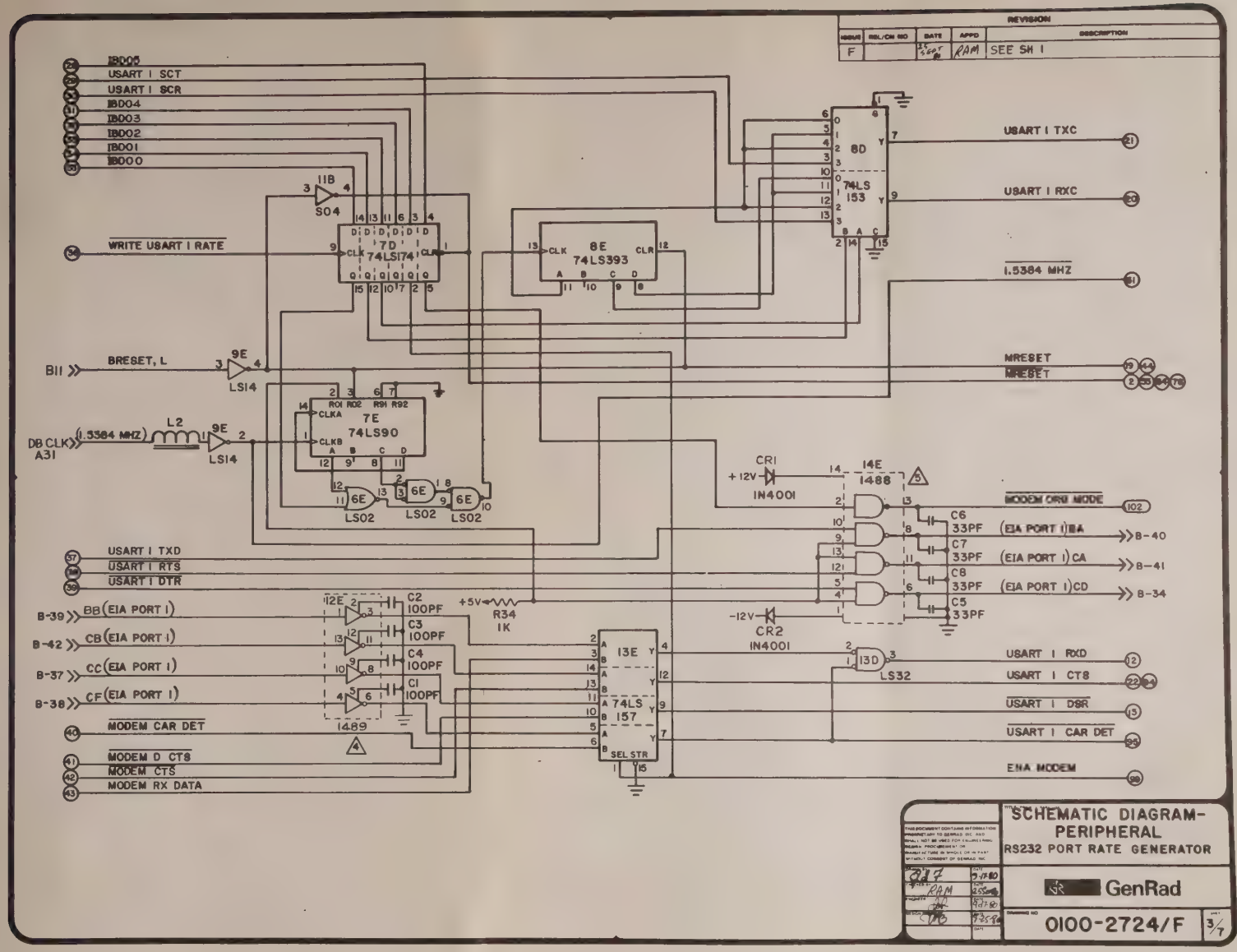
SCALE

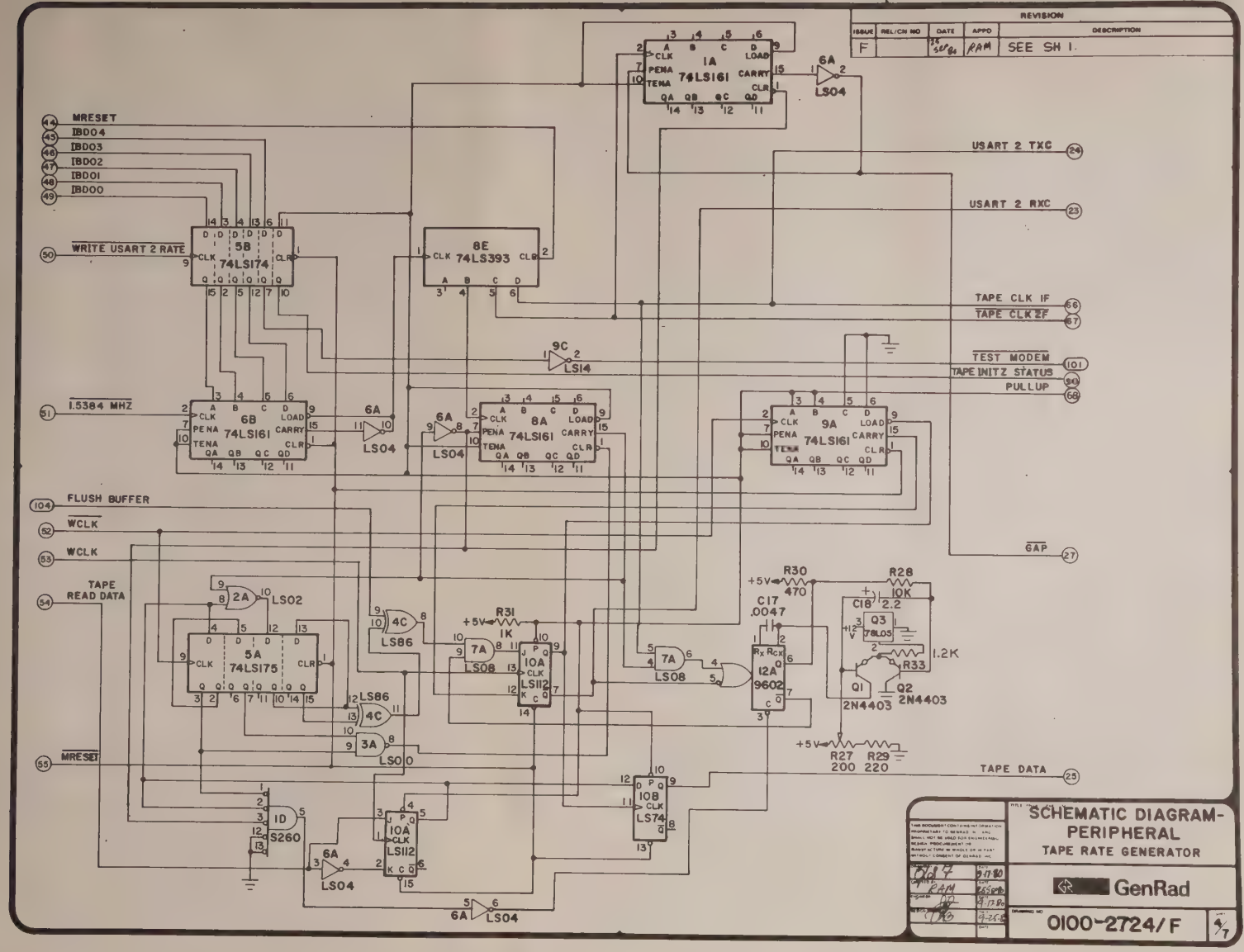
SHEET 6 OF 6

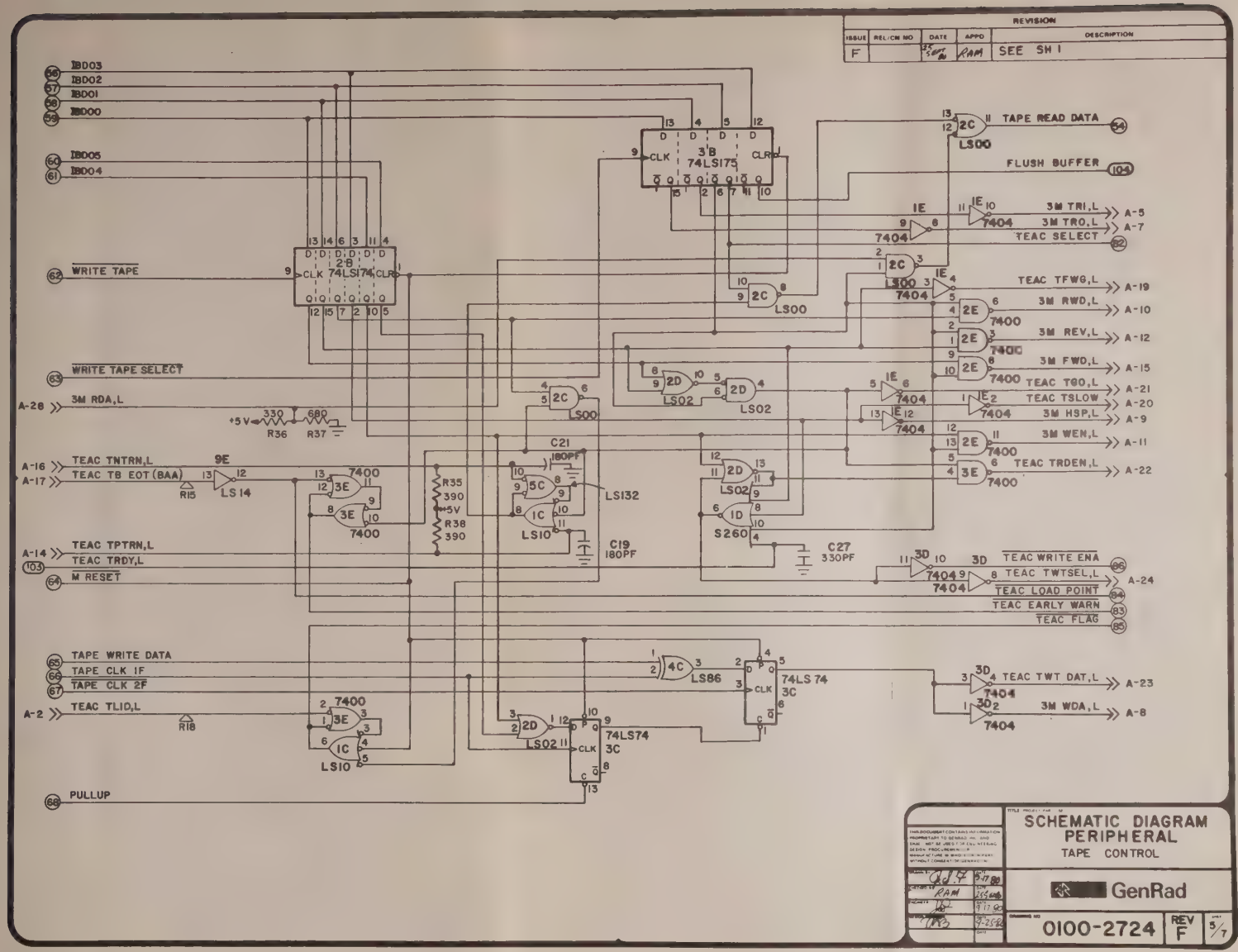
REVISION				
ISSUE	REL CN NO	DATE	APPD	DESCRIPTION
D		2-6-78		REVISED & REDRN TO DEBUG MASTER
D1		5-31-78		REVISED PER ECO 105
D2		7-10-78		REVISED PER ECO 134
E		11-13-78		REVISED PER ECO 168
F		5-18-79		REVISED PER ECO 252
G		6-12-79		ADD SECTION A-A ECO 316
H		9-12-79		REV UPDATED TO AGREE WITH PL-ECO 328
J		9-20-79	JCB	REV PER ECO 352
I		11 28 79		REDRAWN WITHOUT CHANGE
K		7-3-80	DRS	REV PER ECO 414
K			RAM	REVIEWED & CHANGED PER ENG BOT E2000 BD. 0005

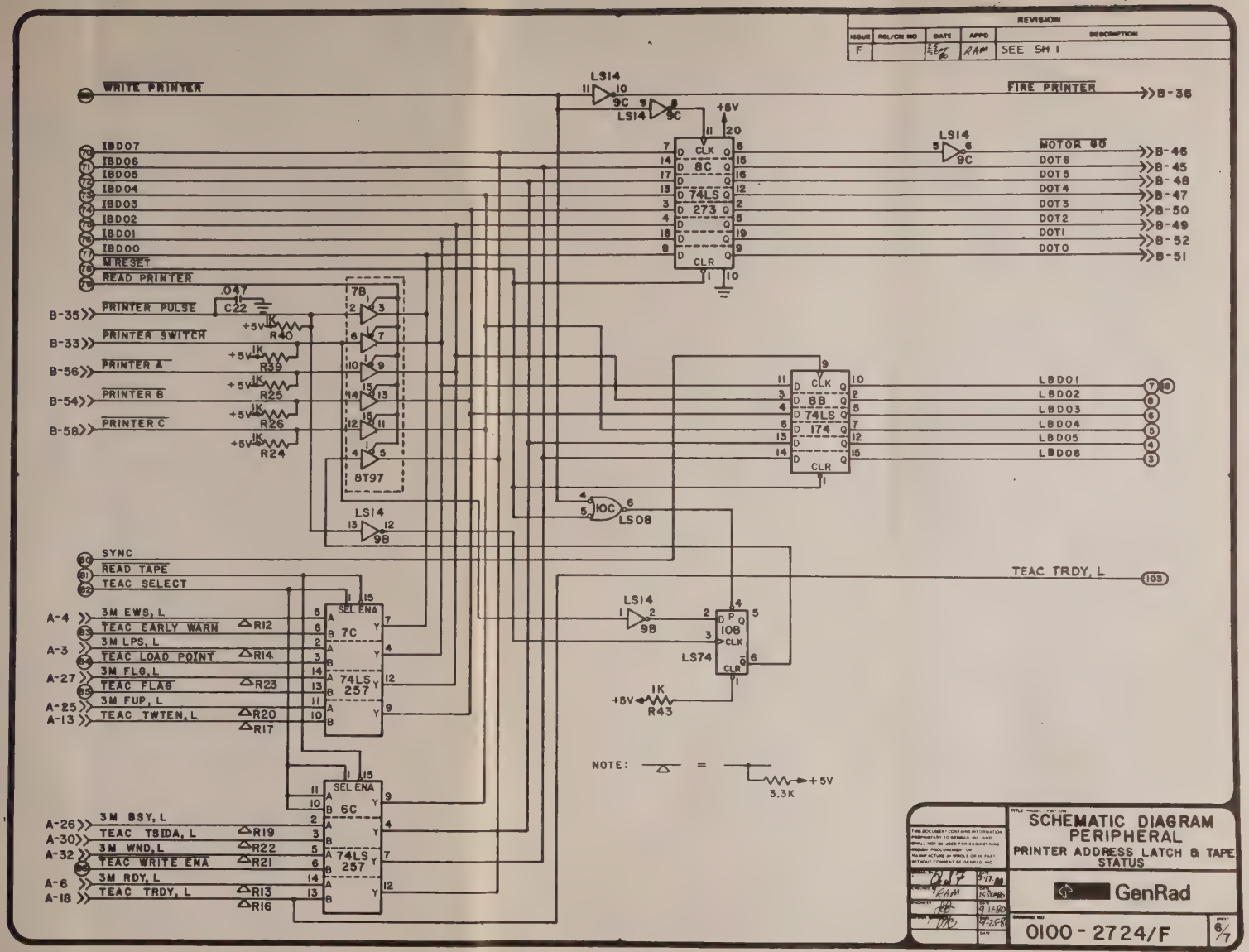
	ASSEMBLY PERIPHERAL BD.
	GenRad PHOENIX ARIZONA 85018
	0100-2724 / K
	1/1

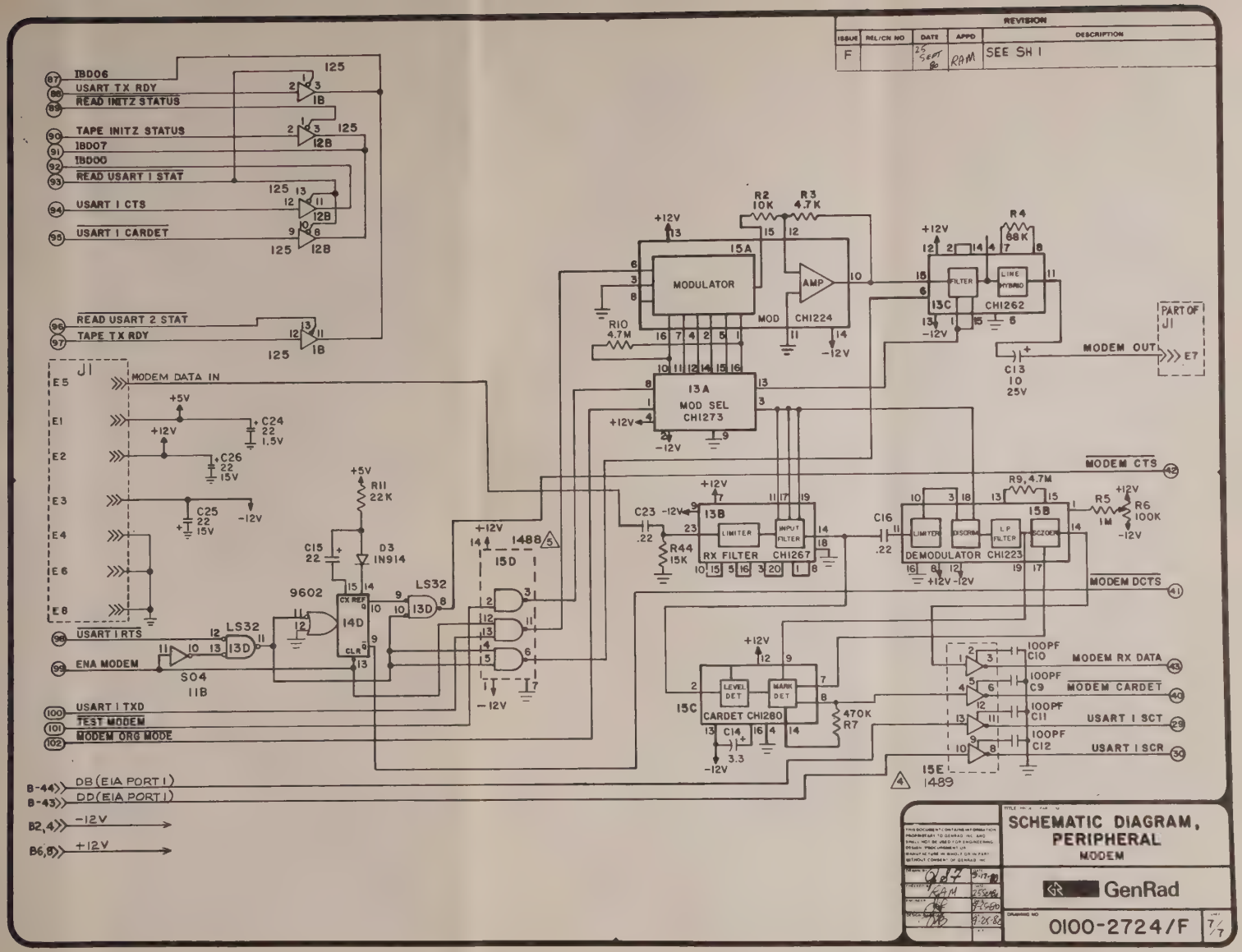

REVISION
ISSUE | REL CN NO | DATE | APPD | DESCRIPTION
F | | 25 SEPT 80 | RAM | SEE SH. 1
A50,52,54,56,58,60 +5
C15 22µf 15V
.1
+5V C28-C85 (58 PLACES)
A53,57 B1,5,9,10,12-14 GND
A-48 BD07
A-46 BD06
A-44 BD05
A-42 BD04
A-40 BD03
A-38 BD02
A-36 BD01
A-34 BD00
8T28 5E
8T28 4E
D/E R/E
ENA BUS IN
USART 1 RXD
CS USART 1
CS USART 2
USART1DSR
DIN
WRITE USART
LBD01
MRESET
USART 1 RXC
USART 1 TXC
USART 1 CTS
USART 2 RXC
USART 2 TXC
TAPE DATA
GAP
BX2, L
BX4, L
B-03
A-55
5C LS132
9C LS14
9C LS14
4D 8251
6D 8251
GND=PIN 4 +5=PIN 26
RESET
74LS92
11B S04
IBD07
IBD06
IBD05
IBD04
IBD03
IBD02
IBD01
IBD00
USART 1 TXD
USART TX RDY
19 TAPE WRITE DATA
15 TAPE TX RDY
USART 1 RTS
USART 1 DTR
BX2
BX4
WCLK
WCLK
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS ±5%, 1/4W.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. DELETED
1489 DIP MAY BE 75189A.
1488A DIP MAY BE 75188.
SCHEMATIC
PERIPHERAL
USART & TEST MUX
GenRad
0100-2724/F
2/7


REVISION
F
SEE SH 1
IBD05
USART I SCT
USART I SCR
IBD04
IBD03
IBD02
IBD01
IBD00
WRITE USART I RATE
11B
S04
7D
74LS174
8E
74LS393
8D
74LS 153
USART I TXC
USART I RXC
1.5384 MHZ
MRESET
MRESET
BRESET, L
9E
LS14
DB CLK
A31
(1.5384 MHZ)
L2
7E
74LS90
6E
LS02
CR1
+12V
IN4001
14E
1488
MODEM CRU MODE
C6
33PF
(EIA PORT I)BA
C7
33PF
(EIA PORT I)CA
C8
33PF
(EIA PORT I)CD
C5
33PF
-12V
CR2
IN4001
USART I TXD
USART I RTS
USART I DTR
BB(EIA PORT I)
CB(EIA PORT I)
CC(EIA PORT I)
CF(EIA PORT I)
12E
C2
100PF
C3
100PF
C4
100PF
C1
100PF
1489
+5V
R34
1K
13E
74LS
157
SEL STR
13D
LS32
USART I RXD
USART I CTS
USART I DSR
USART I CAR DET
ENA MODEM
MODEM CAR DET
MODEM D CTS
MODEM CTS
MODEM RX DATA
SCHEMATIC DIAGRAM-
PERIPHERAL
RS232 PORT RATE GENERATOR
GenRad
0100-2724/F
3/7

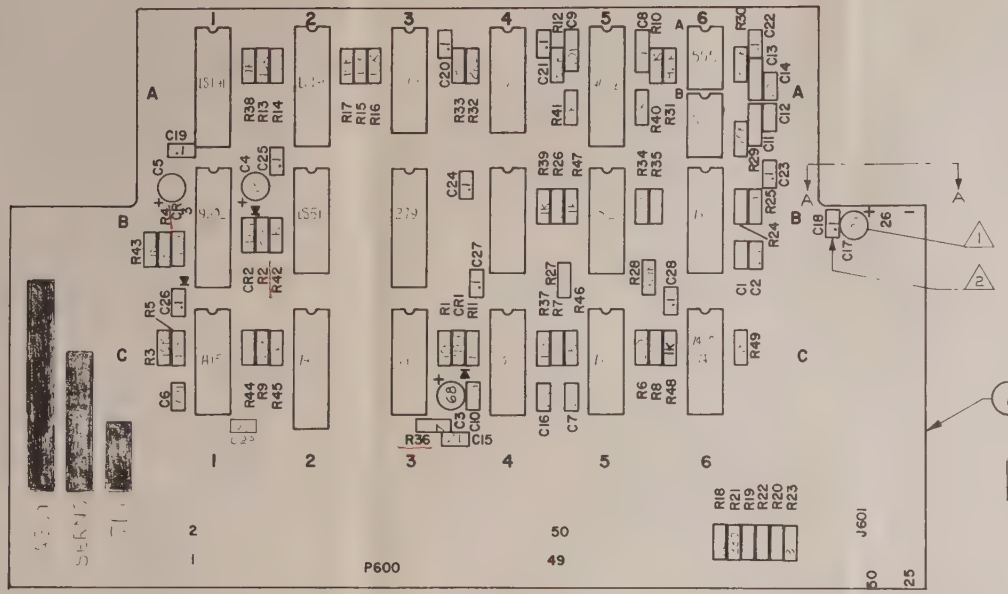

REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
F | | 3/5/80 | RAM | SEE SH 1.
MRESET
IBD04
IBD03
IBD02
IBD01
IBD00
WRITE USART 2 RATE
1.5384 MHZ
FLUSH BUFFER
WCLK
WCLK
TAPE READ DATA
MRESET
1A 74LS161
6A LS04
8E 74LS393
5B 74LS174
6B 74LS161
8A 74LS161
9A 74LS161
9C LS14
2A LS02
5A 74LS175
4C LS86
7A LS08
10A LS112
3A LS00
1D LS260
10B LS74
12A 9602
R30 470
R28 10K
C17 .0047
C18 2.2
Q3 TIP105
R33 1.2K
Q1 2N4403
Q2 2N4403
R31 1K
R27 200
R29 220
USART 2 TXC
USART 2 RXC
TAPE CLK IF
TAPE CLK 2F
TEST MODEM
TAPE INITZ STATUS
PULLUP
GAP
TAPE DATA
SCHEMATIC DIAGRAM-PERIPHERAL
TAPE RATE GENERATOR
GenRad
0100-2724/F


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
F | | 23 Sept 80 | RAM | SEE SH 1
IBD03
IBD02
IBD01
IBD00
IBD05
IBD04
WRITE TAPE
WRITE TAPE SELECT
3M RDA,L
TEAC TNTRN,L
TEAC TB EOT(BAA)
TEAC TPTRN,L
TEAC TRDY,L
M RESET
TAPE WRITE DATA
TAPE CLK 1F
TAPE CLK 2F
TEAC TLID,L
PULLUP
+5V
330
680
R36
R37
R35 390
R38 390
C21 180PF
C19 180PF
C27 330PF
R15
R18
3B 74LS175
2B 74LS74
LS00
LS02
LS14
LS10
LS132
S260
LS86
74LS74 3C
7400
7404
TAPE READ DATA
FLUSH BUFFER
3M TRI,L
3M TRO,L
TEAC SELECT
TEAC TFWG,L
3M RWD,L
3M REV,L
3M FWD,L
TEAC T00,L
TEAC TSLOW
3M HSP,L
3M WEN,L
TEAC TRDEN,L
TEAC WRITE ENA
TEAC TWTSEL,L
TEAC LOAD POINT
TEAC EARLY WARN
TEAC FLAG
TEAC TWT DAT,L
3M WDA,L
A-5
A-7
A-19
A-10
A-12
A-15
A-21
A-20
A-9
A-11
A-22
A-24
A-23
A-8
SCHEMATIC DIAGRAM
PERIPHERAL
TAPE CONTROL
GenRad
0100-2724
REV F
5/7


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
F | | | RAM | SEE SH 1
WRITE PRINTER
FIRE PRINTER
B-36
IBD07
IBD06
IBD05
IBD04
IBD03
IBD02
IBD01
IBD00
W RESET
READ PRINTER
PRINTER PULSE
PRINTER SWITCH
PRINTER A
PRINTER B
PRINTER C
B-35
B-33
B-56
B-54
B-58
.047 C22
1K R40
1K R39
1K R25
1K R26
1K R24
+5V
8T97
LS14 9C
LS14 9B
LS14 10C
LS08
8C 74LS 273 CLK CLR
8B 74LS 174 CLK CLR
MOTOR 60
DOT6
DOT5
DOT4
DOT3
DOT2
DOT1
DOT0
B-46
B-45
B-48
B-47
B-50
B-49
B-52
B-51
LBD01
LBD02
LBD03
LBD04
LBD05
LBD06
SYNC
READ TAPE
TEAC SELECT
TEAC TRDY, L
103
3M EWS, L
TEAC EARLY WARN
3M LPS, L
TEAC LOAD POINT
3M FLG, L
TEAC FLAG
3M FUP, L
TEAC TWTEN, L
A-4
A-3
A-27
A-25
A-13
R12
R14
R23
R20
R17
7C 74LS 257 SEL ENA
3M BSY, L
TEAC TSIDA, L
3M WND, L
TEAC WRITE ENA
3M RDY, L
TEAC TRDY, L
A-26
A-30
A-32
A-6
A-18
R19
R22
R21
R13
R16
6C 74LS 257 SEL ENA
LS74 10B
1K R43
NOTE:
3.3K
SCHEMATIC DIAGRAM
PERIPHERAL
PRINTER ADDRESS LATCH & TAPE STATUS
GenRad
0100-2724/F
6/7


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
F | | 26 SEPT 80 | RAM | SEE SH 1
IBD06
USART TX RDY
READ INITZ STATUS
TAPE INITZ STATUS
IBD07
IBD00
READ USART I STAT
USART I CTS
USART I CARDET
READ USART 2 STAT
TAPE TX RDY
J1
MODEM DATA IN
+5V
+12V
C24 22 1.5V
C26 22 15V
C25 22 15V
-12V
USART I RTS
ENA MODEM
S04
11B
LS32
13D
9602
14D
CX REG
CLR
R11 22K
C15 22
D3 IN914
1488
15D
USART I TXD
TEST MODEM
MODEM ORG MODE
DB (EIA PORT 1)
DD (EIA PORT 1)
-12V
+12V
R2 10K
R3 4.7K
15A
MODULATOR
AMP
MOD CHI224
R10 4.7M
13A
MOD SEL CHI273
R4 68K
FILTER
LINE HYBRID
13C CHI262
C13 10 25V
MODEM OUT
PART OF J1
13B
LIMITER
INPUT FILTER
RX FILTER CHI267
C23 .22
R44 15K
R9, 4.7M
R5 1M
R6 100K
LP FILTER
DISCRIM
SCZOER
DEMODULATOR CHI223
C16 .22
MODEM CTS
MODEM DCTS
15C
LEVEL DET
MARK DET
CARDET CHI280
C14 3.3
470K R7
100PF C10
100PF C9
100PF C11
100PF C12
MODEM RX DATA
MODEM CARDET
USART I SCT
USART I SCR
15E 1489
SCHEMATIC DIAGRAM, PERIPHERAL
MODEM
GenRad
0100-2724/F
7/7

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ADDED C 3 AND ITEM 1 TO F/D	3-[illegible]-78	
	B	REVISED PER ECO [illegible]	7-10-78	
	B_1	REVISED PER ECO 153	10-4-78	
	C	REVISED PER ECO 402 BLW	4-29-80	
	–	REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005	25 SEPT 80	RAM



TAPE DRIVE INTERFACE
0100-0736

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
. XX ± ±
XXX ±

CONTRACT NO

APPROVALS	DATE
[illegible] L DALES	9-17-80
[illegible] RAM	25 SEPT 80
[illegible]	[illegible]
[illegible]	9-25-80

MATERIAL

FINISH

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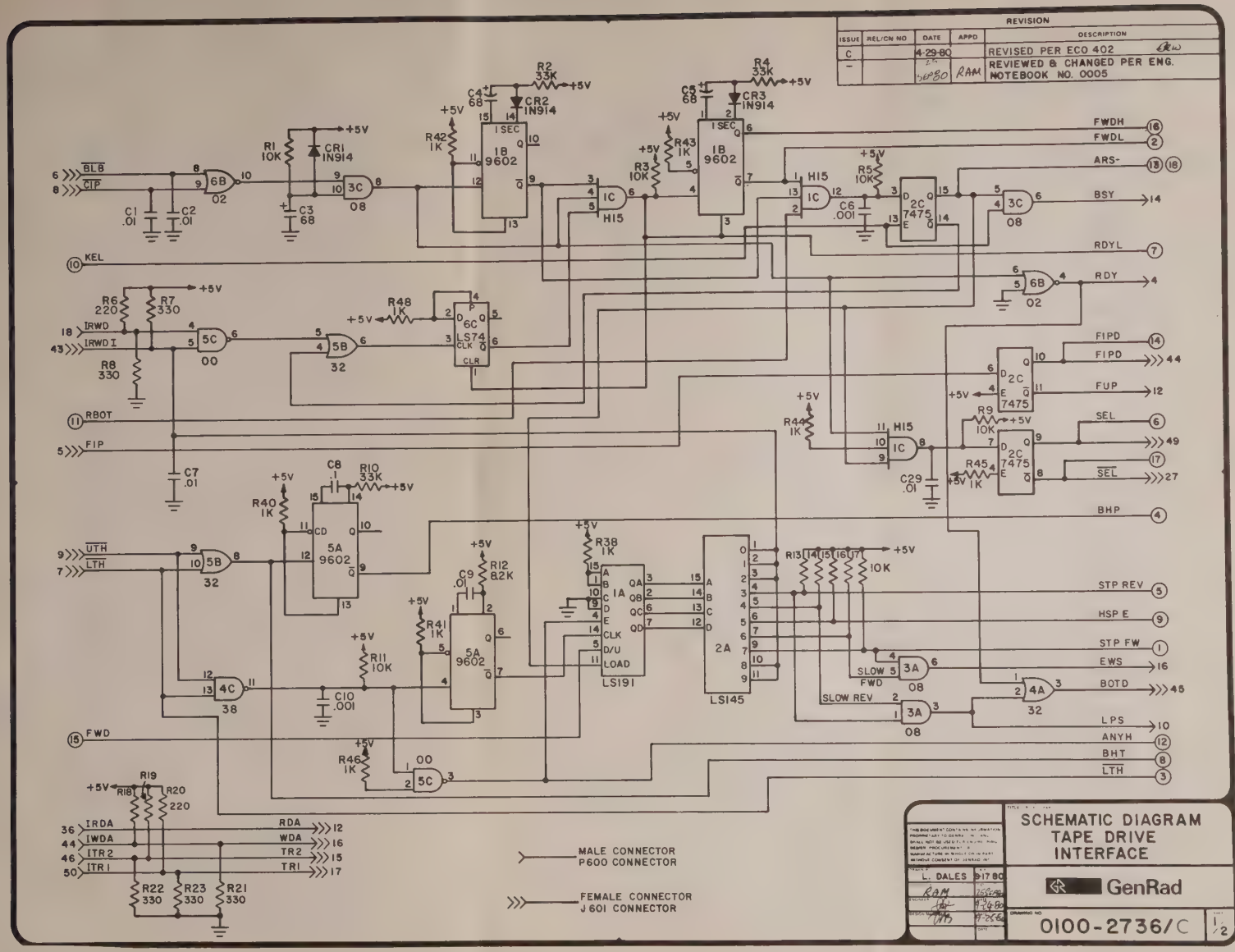
ASSEMBLY
TAPE DRIVE INTERFACE

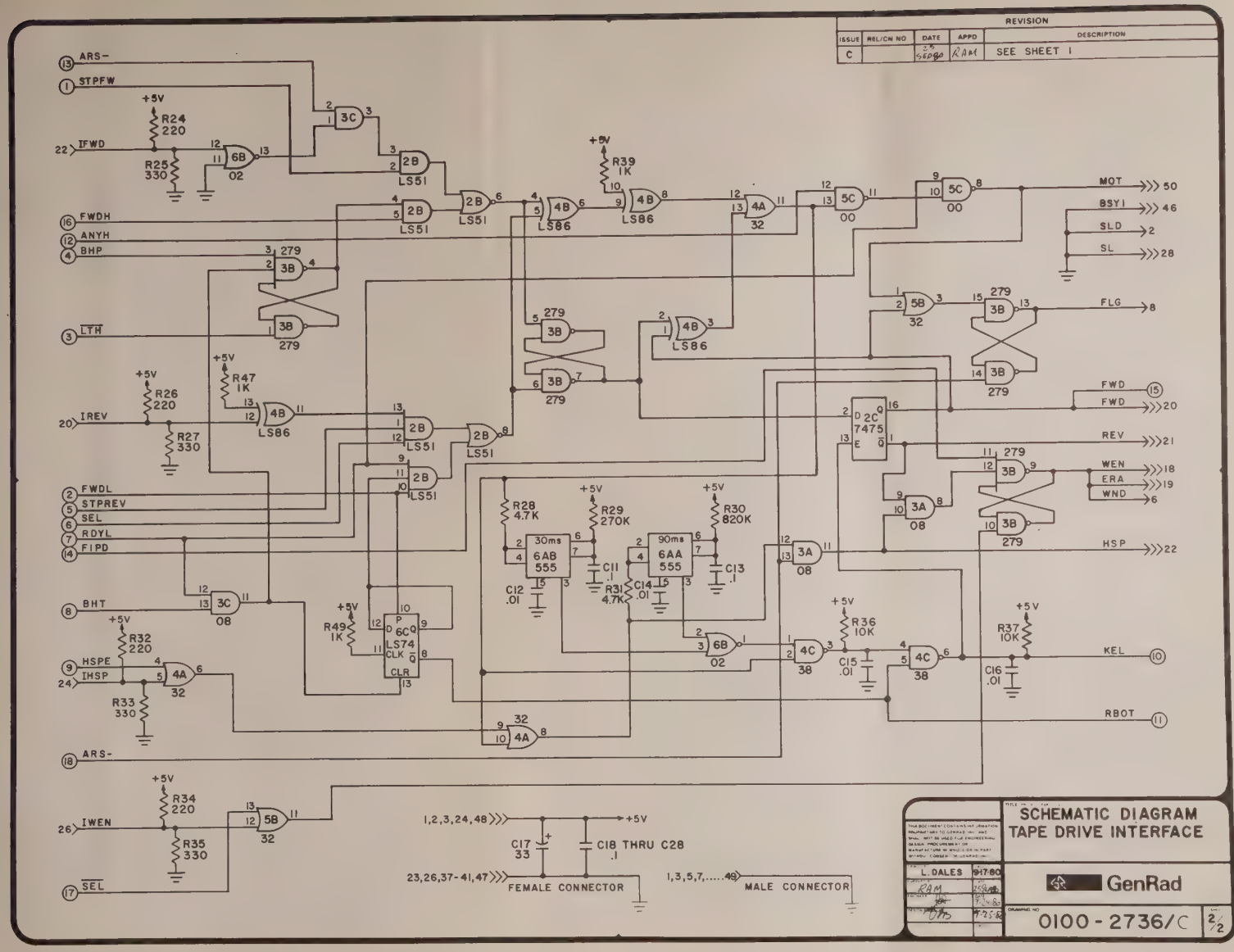
SIZE	CODE IDENT NO	DRAWING NO	REV
C		0100-2736	C

SCALE | SHEET 1 OF 1

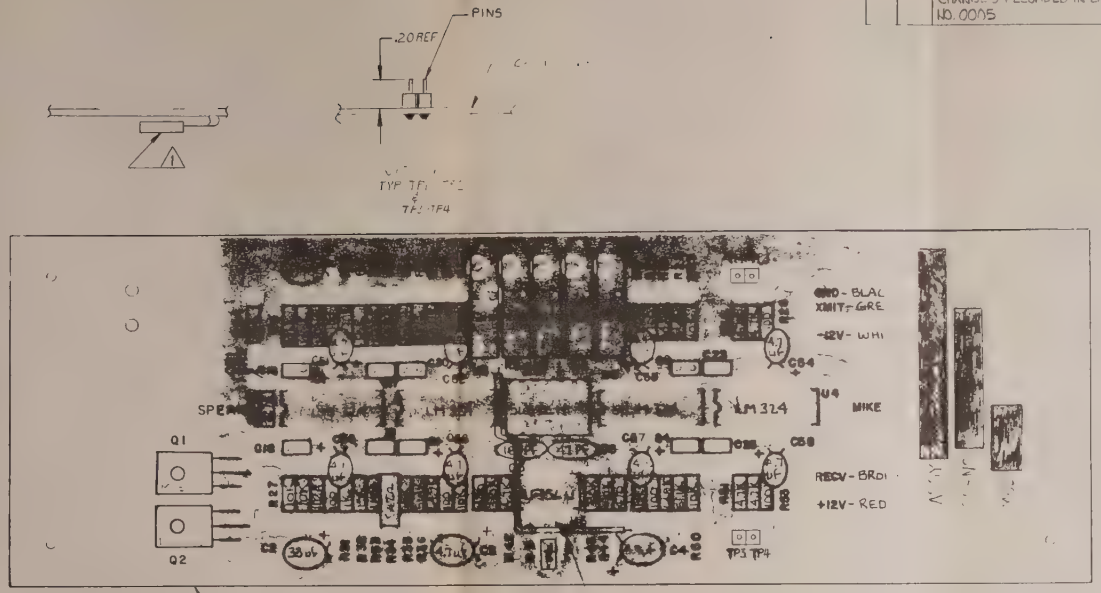
NEXT ASSY	USED ON
APPLICATION	DO NOT SCALE DRAWING

⚠2 MOUNT C18 [illegible] ABOVE PCB
⚠1 MOUNT C17 [illegible] ABOVE PCB
NOTES:


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
C | | 4-29-80 | | REVISED PER ECO 402
- | | 5-6-80 | RAM | REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005
SCHEMATIC DIAGRAM
TAPE DRIVE
INTERFACE
L. DALES 9/7/80
GenRad
0100-2736/C
1/2
MALE CONNECTOR
P600 CONNECTOR
FEMALE CONNECTOR
J 601 CONNECTOR
BLB
CIP
KEL
IRWD
IRWDI
RBOT
FIP
UTH
LTH
FWD
IRDA
IWDA
ITR2
ITR1
FWDH
FWDL
ARS-
BSY
RDYL
RDY
FIPD
FIPD
FUP
SEL
SEL
BHP
STP REV
HSP E
STP FW
EWS
BOTD
LPS
ANYH
BHT
LTH
RDA
WDA
TR2
TRI
SLOW FWD
SLOW REV
LS191
LS145


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
C | | 28 SEP 80 | RAM | SEE SHEET 1
ARS-
STPFW
IFWD
FWDH
ANYH
BHP
LTH
IREV
FWDL
STPREV
SEL
RDYL
FIPD
BHT
HSPE
IHSP
IWEN
SEL
ARS-
+5V
R24 220
R25 330
R26 220
R27 330
R32 220
R33 330
R34 220
R35 330
R47 1K
R49 1K
R28 4.7K
R29 270K
R30 820K
R31 4.7K
R36 10K
R37 10K
R39 1K
C11 .1
C12 .01
C13 .1
C14 .01
C15 .01
C16 .01
C17 33
C18 THRU C28 .1
30ms 6AB 555
90ms 6AA 555
LS51
LS86
LS74
7475
MOT
BSY1
SLD
SL
FLG
FWD
REV
WEN
ERA
WND
HSP
KEL
RBOT
1,2,3,24,48
23,26,37-41,47
FEMALE CONNECTOR
1,3,5,7,.....49
MALE CONNECTOR
SCHEMATIC DIAGRAM
TAPE DRIVE INTERFACE
L.DALES 9/7/80
RAM 9/24/80
GenRad
0100-2736/C
2/2

ZONE	LTR		DATE	APPROVED
	F	[illegible] 298	6/5/7[illegible]	[illegible]
	G	REVISED PER ECO 323	7/21/77	J Scully
	H	DWG NO WAS 0100-2738/S DWG NO CHANGED FOR [illegible] INTERFACE BD LEVEL TO 'H' TO TRACK WITH NEXT ASSY NO-ALSO CHANGED AT THIS TIME. CHANGES RECORDED IN ENG NOTEBOOK NO. 0005	7/8/80	RAM



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
± XX ± XXX

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
[illegible] SILER	9-16-[illegible]
[illegible] KRUL	[illegible]

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CIRCUIT CARD ASSEMBLY
MODEM INTERFACE
PSP

SIZE C | DRAWING 0100 1738 | REV. H

SCALE | SHEET 1 of 1

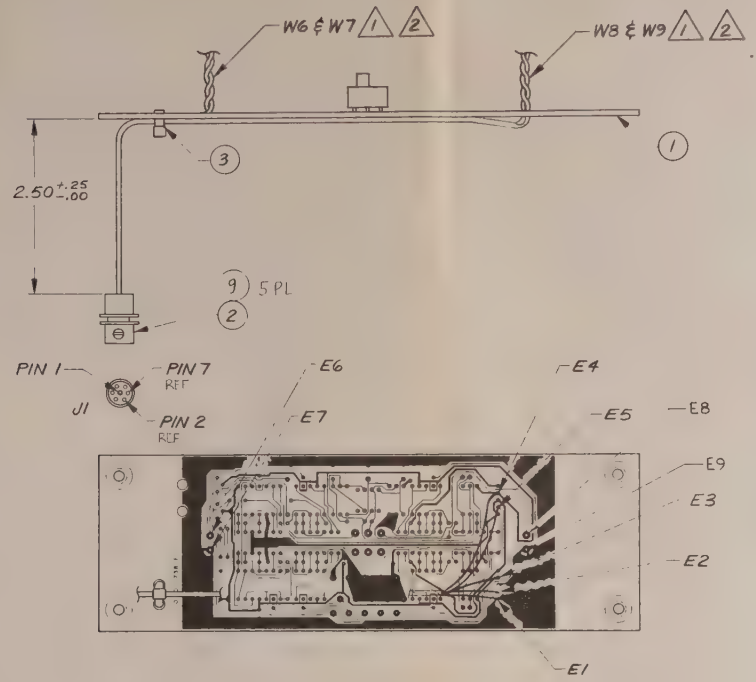
NEXT ASSY	USED ON
APPLICATION	

2. C16 - C25 ARE [illegible]

⚠ FOR LEAD [illegible] APPROX [illegible] WITH METAL SURFACE OF ELECTROLYTIC FOR MTG BOARD

NOTES:

REVISION				
ISSUE	REL/CN NO	DATE	APPD	DESCRIPTION
H		9-10-80	RAM	DWG NO. WAS 0100-3738/E. DWG NO. CHANGED FOR SYSTEM UNIFORMITY. REV TO "H" TO AVOID CONFLICT WITH 0100-2738/G WHICH BECAME 0100-1738/H FOR SYSTEM UNIFORMITY CHANGES RECORDED IN ENG NOTEBOOK NO. 0005



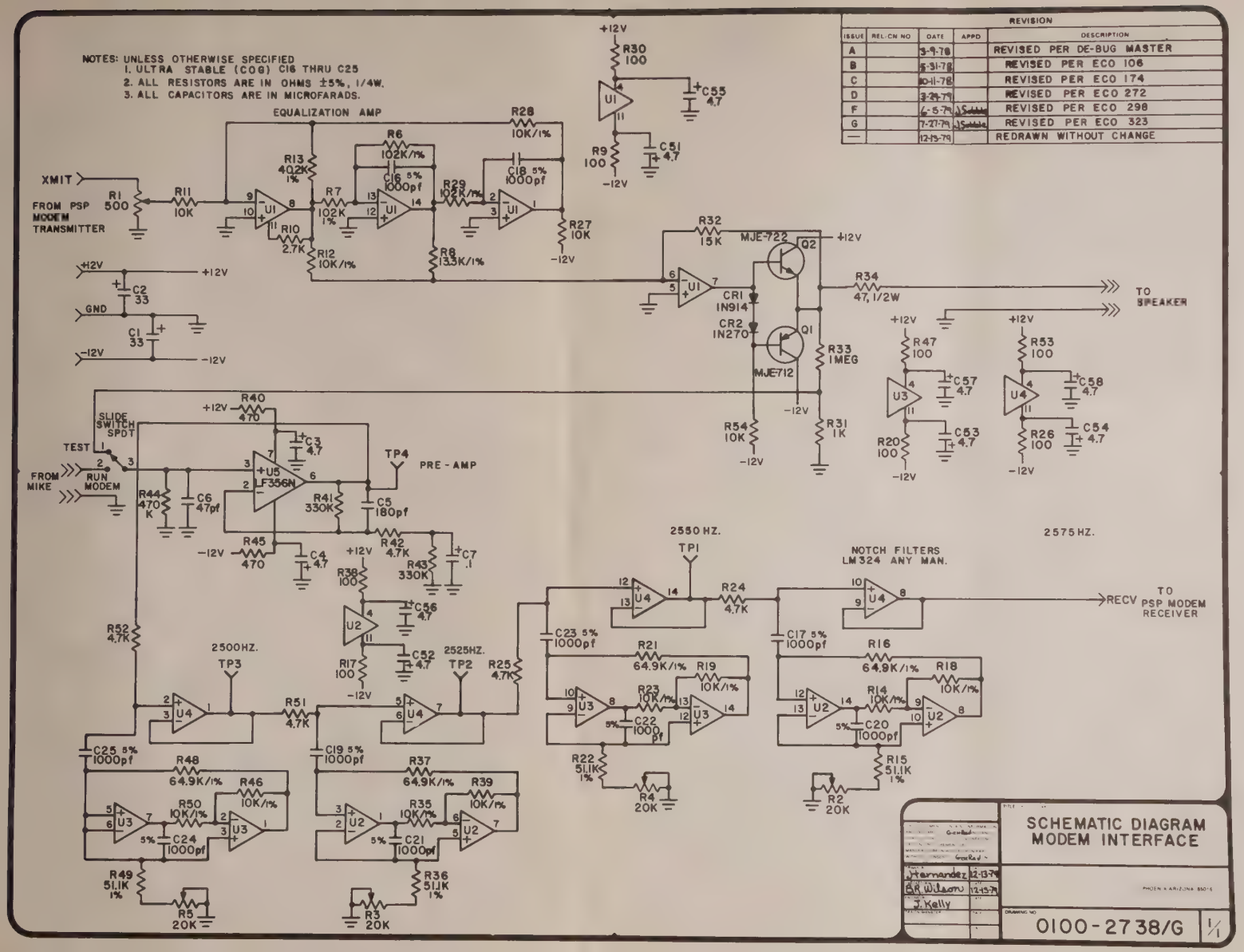
WIRE LIST							
WIRE NO.	TERMINATION FROM	TERMINATION TERM	WIRE AWG	WIRE COLOR	WIRE CUT LENGTH	TERMINATION TO	TERMINATION TERM
W1	J1-1	IT-9	22	BLK	8 IN.	E1	SOLDER
W2	J1-2	↓	↓	GRN	8 IN.	E2	↑
W3	J1-3	↓	↓	WHT	8 IN.	E3	↑
W4	J1-4	↓	↓	RED	9 IN.	E4	↑
W5	J1-5	IT-9	↓	BRN	9 IN.	E5	↑
W6	2	SOLDER	↓	WHT	4 AFTER	E6	↑
W7	2	↓	↓	BLK	4 TWIST	E7	↑
W8	2	↓	↓	RED	4 AFTER	E8	↑
W9	2	SOLDER	22	BLK	4 AFTER	E9	SOLDER

2 LOOSE ENDS OF W6-W9 ARE TERMINATED AT NEXT ASSY

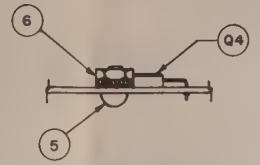
1 MAKE TWISTED PAIR, 4 TURNS PER INCH

NOTES:

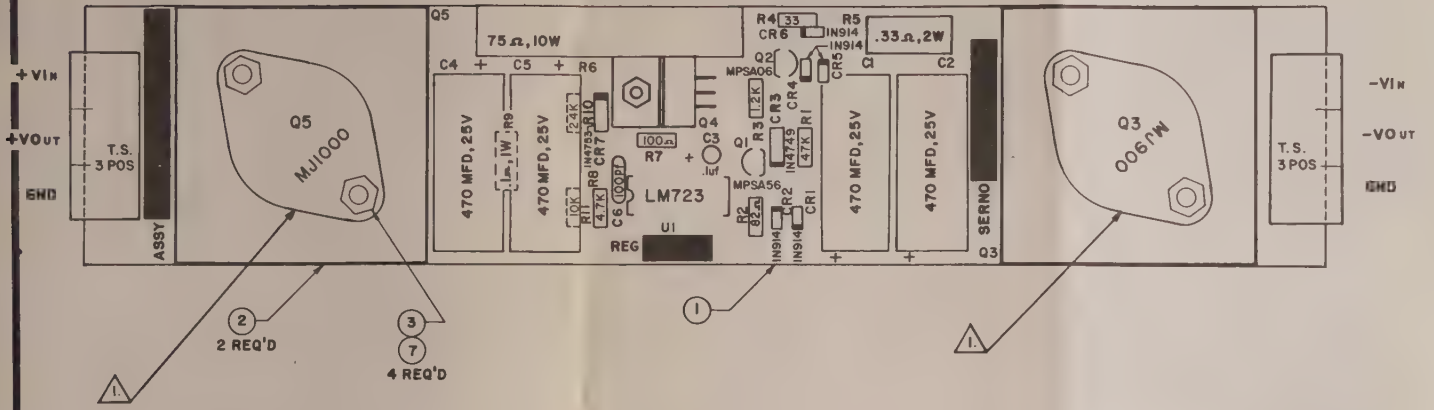
TOL: 2 PLC ± 02 3 PLC ± 010	CIRCUIT CARD ASSY, MODEM INTERFACE PSP	
J5 FROMM 9-10-80 RAM	GenRad PHOENIX ARIZONA 85016	
	0100-2738/H	1/1


NOTES: UNLESS OTHERWISE SPECIFIED
1. ULTRA STABLE (COG) C16 THRU C25
2. ALL RESISTORS ARE IN OHMS ±5%, 1/4W.
3. ALL CAPACITORS ARE IN MICROFARADS.
REVISION
ISSUE | REL'CN NO | DATE | APPD | DESCRIPTION
A | | 3-9-78 | | REVISED PER DE-BUG MASTER
B | | 5-31-78 | | REVISED PER ECO 106
C | | 10-11-78 | | REVISED PER ECO 174
D | | 3-29-79 | | REVISED PER ECO 272
F | | 6-5-79 | | REVISED PER ECO 298
G | | 7-27-79 | | REVISED PER ECO 323
— | | 12-13-79 | | REDRAWN WITHOUT CHANGE
EQUALIZATION AMP
XMIT
FROM PSP MODEM TRANSMITTER
R1 500
R11 10K
R13 40.2K 1%
R6 102K/1%
C16 5% 1000pf
R7 102K 1%
R10 2.7K
R12 10K/1%
R8 13.3K/1%
R29 102K/1%
C18 5% 1000pf
R28 10K/1%
R27 10K
R30 100
C55 4.7
R9 100
C51 4.7
R32 15K
MJE-722 Q2
CR1 IN914
CR2 IN270
Q1 MJE712
R33 1MEG
R34 47, 1/2W
TO SPEAKER
R54 10K
R31 1K
R47 100
C57 4.7
R20 100
C53 4.7
R53 100
C58 4.7
R26 100
C54 4.7
C2 33
C1 33
GND
SLIDE SWITCH SPDT
TEST
RUN MODEM
FROM MIKE
R40 470
C3 4.7
TP4
PRE-AMP
LF356N
R44 470 K
C6 47pf
R41 330K
C5 180pf
R45 470
C4 4.7
R42 4.7K
R43 330K
C7 .1
R38 100
C56 4.7
R52 4.7K
2500HZ.
TP3
C52 4.7
R17 100
2525HZ.
TP2
R25 4.7K
R51 4.7K
2550 HZ.
TP1
2575HZ.
NOTCH FILTERS LM324 ANY MAN.
R24 4.7K
C23 5% 1000pf
R21 64.9K/1%
R19 10K/1%
R23 10K/1%
C22 1000 pf
R22 51.1K 1%
R4 20K
C17 5% 1000pf
R16 64.9K/1%
R18 10K/1%
R14 10K/1%
C20 1000pf
R15 51.1K 1%
R2 20K
RECV
TO PSP MODEM RECEIVER
C25 5% 1000pf
R48 64.9K/1%
R46 10K/1%
R50 10K/1%
C24 1000pf
R49 51.1K 1%
R5 20K
C19 5% 1000pf
R37 64.9K/1%
R39 10K/1%
R35 10K/1%
C21 1000pf
R36 51.1K 1%
R3 20K
SCHEMATIC DIAGRAM MODEM INTERFACE
Hernandez 12-13-79
GR Wilson 12-13-79
J. Kelly
0100-2738/G
1/1

REVISION				
ISSUE	REL CN NO	DATE	APPD	DESCRIPTION
B		2-8-78		REVISED PER DEBUG MASTER
—		11-27-79		REDRAWN WITHOUT REV CHANGE
C		2-22-80		REVISED PER ECO 390
D		7-25-80	(GD)	REV PER ECO 413
—		26 Sept 86	RAM	REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005



DETAIL, Q4 MOUNTING



1. APPLY SILICONE HEAT SINK COMPOUND (ITEM 4) BEFORE INSTALLING.

NOTES: UNLESS OTHERWISE SPECIFIED

DRAWN	L. DALES	9-18-80
CHECKED	RAM	9-26-80
ENGINEER		
MFG		
QUALITY		

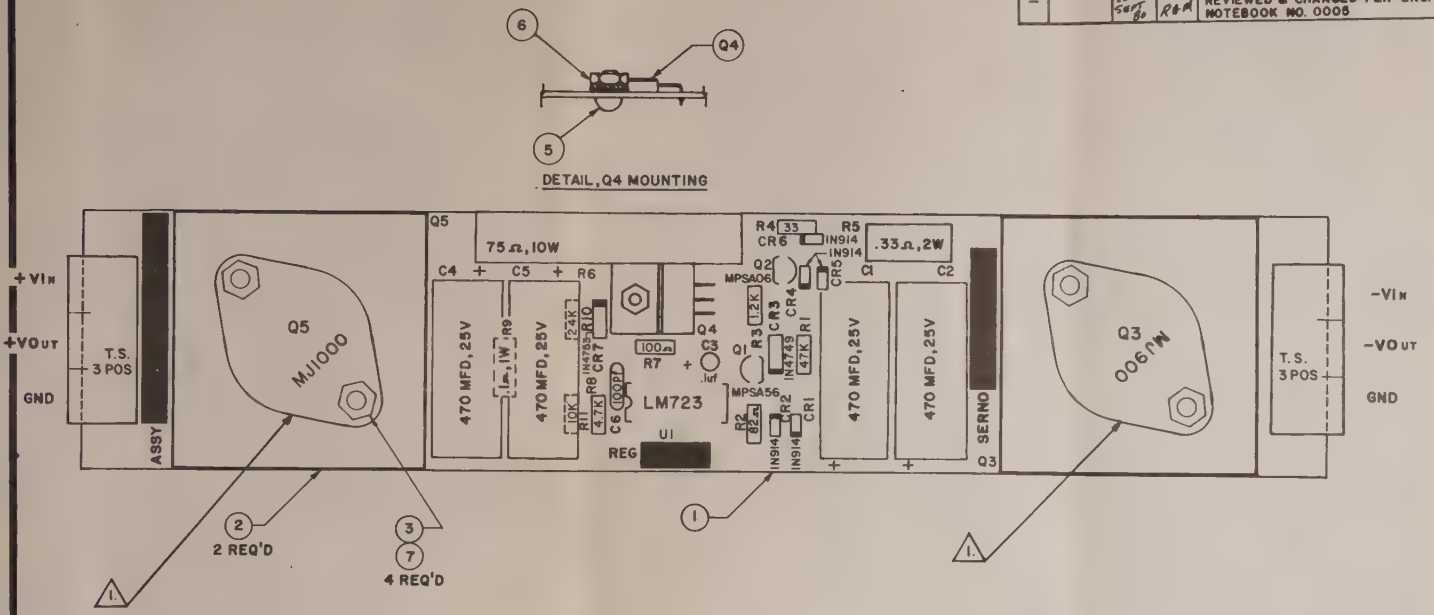
ASSEMBLY
24V REGULATOR

GenRad

0100-2719/D

1/1

REVISION				
ISSUE	REL CN NO	DATE	APPD	DESCRIPTION
B		2-8-79		REVISED PER DEBUG MASTER
—		11-27-79		REDRAWN WITHOUT REV CHANGE
C		2-22-80		REVISED PER ECO 390
D		7-25-80	BDL	REV PER ECO 413
—		26 SEPT 80	R&M	REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005



1. APPLY SILICONE HEAT SINK COMPOUND (ITEM 4) BEFORE INSTALLING.

NOTES: UNLESS OTHERWISE SPECIFIED

DRAWN	L. DALES	9-18-80
CHECKED	RAM	9-26-80
ENGR APPR		9-26-80
MFG APPR		9-26-80

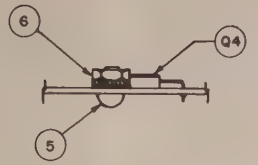
ASSEMBLY
24V REGULATOR

GenRad

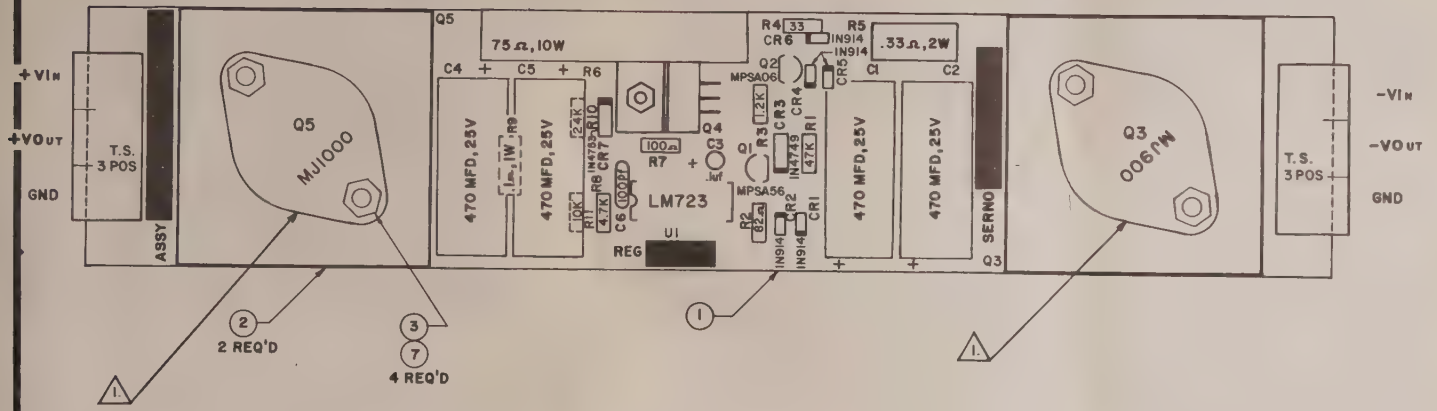
DRAWING NO 0100-2719/D

SHT 1/1

REVISION				
ISSUE	REL CN NO	DATE	APPD	DESCRIPTION
B		2-8-78		REVISED PER DEBUG MASTER
—		11-27-78		REDRAWN WITHOUT REV CHANGE
C		2-22-80		REVISED PER ECO 390
D		7-25-80	GDA	REV PER ECO 413
—		26 Sept 80	RAM	REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005



DETAIL, Q4 MOUNTING



1. APPLY SILICONE HEAT SINK COMPOUND (ITEM 4) BEFORE INSTALLING.

NOTES: UNLESS OTHERWISE SPECIFIED

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO GENRAD INC. AND SHALL NOT BE USED FOR ENGINEERING OR MANUFACTURE IN WHOLE OR IN PART WITHOUT CONSENT OF GENRAD INC.

DRAWN	L. DALES	9-18-80
ENGR	RAM	10-6-80
MFG		9-26-80
QUAL		9-26-80

ASSEMBLY
24V REGULATOR

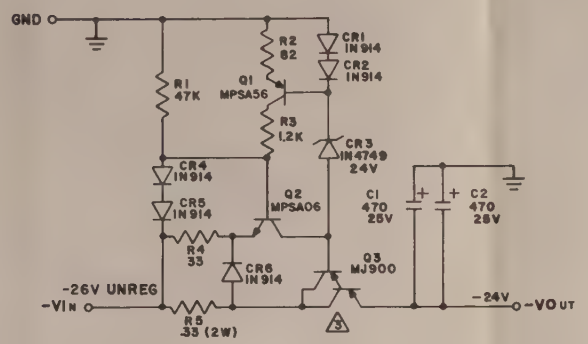
GenRad

DRAWING NO. 0100-2719/D

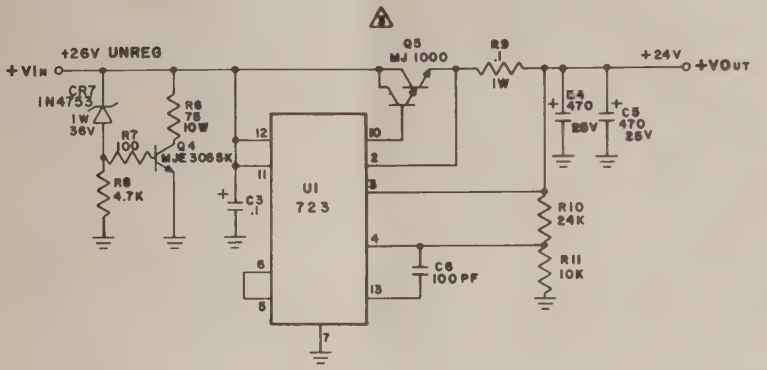
SHT 1/1

REVISIONS				
ECO NO.	REL/CHK NO.	DATE	APPD	DESCRIPTION
-1		2-10-77		SEE HISTORY FILE
A		2-10-77		470 CAPS WERE 500
B		2-10-78		UPDATE REV (DESIGN MASTER)
—		2-20-79	-	REDRAWN WITHOUT CHANGE
C		1-22-80		REVISED PER ECO 390
D		7-25-84		REV PER ECO 413
—		25 Sep 86	PAM	REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0006

-24 VOLT, CURRENT LIMITED, REGULATOR



+24 VOLT, CURRENT LIMITED, SHUNT-INPUT, REGULATOR



NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS ± 5%, 1/4 W.
2. ALL CAPACITORS ARE IN MICROFARADS.

3 HEATSINKS REQUIRED FOR THESE TRANSISTORS.

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO GENRAD, INC. AND SHALL NOT BE USED FOR ENGINEERING, DESIGN, PROCUREMENT, OR MANUFACTURE IN WHOLE OR IN PART WITHOUT CONSENT OF GENRAD, INC.

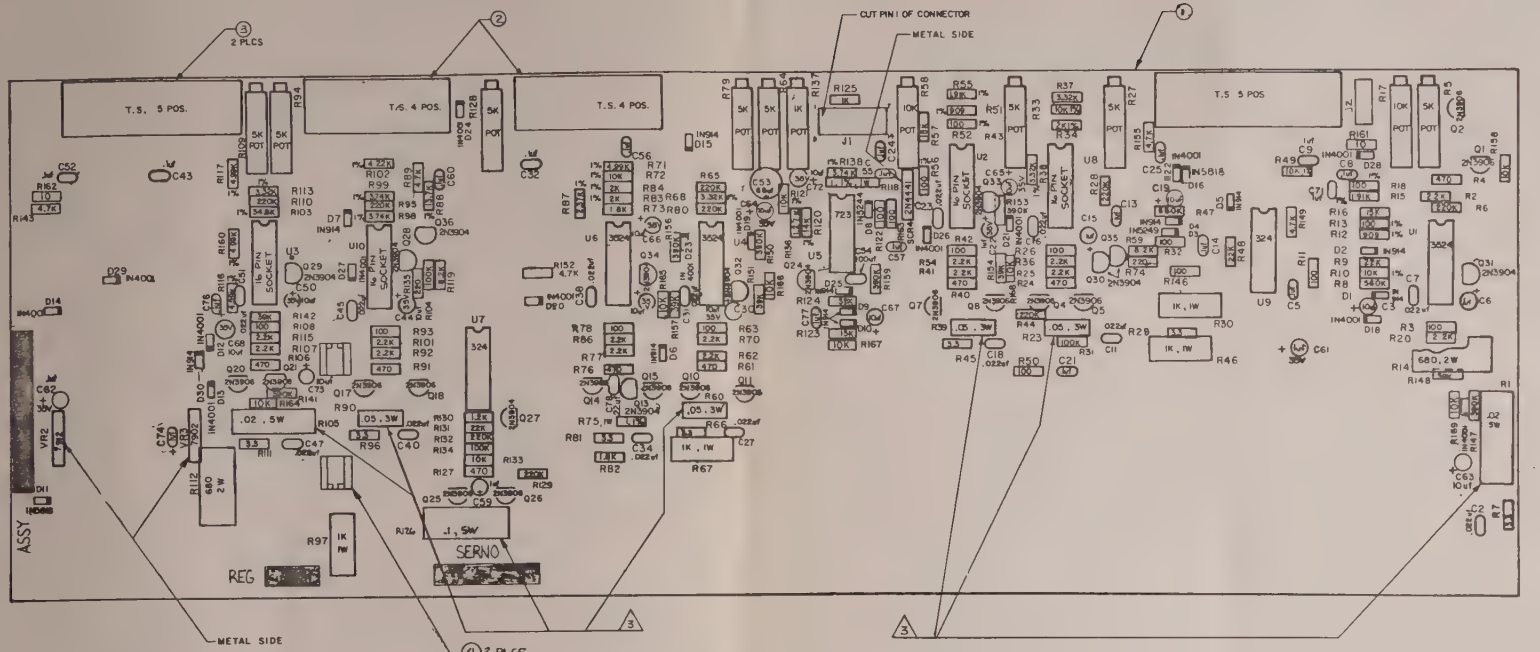
DRAWN	L. DALES	DATE 2-6-80
DESIGNED	R.A.M.	DATE 2-6-80
CHECKED		DATE 9-25-80
APPROVED		DATE 9-25-80

SCHEMATIC DIAGRAM
24V REGULATORS

GenRad

0100-2719 REV D SHEET 1/1

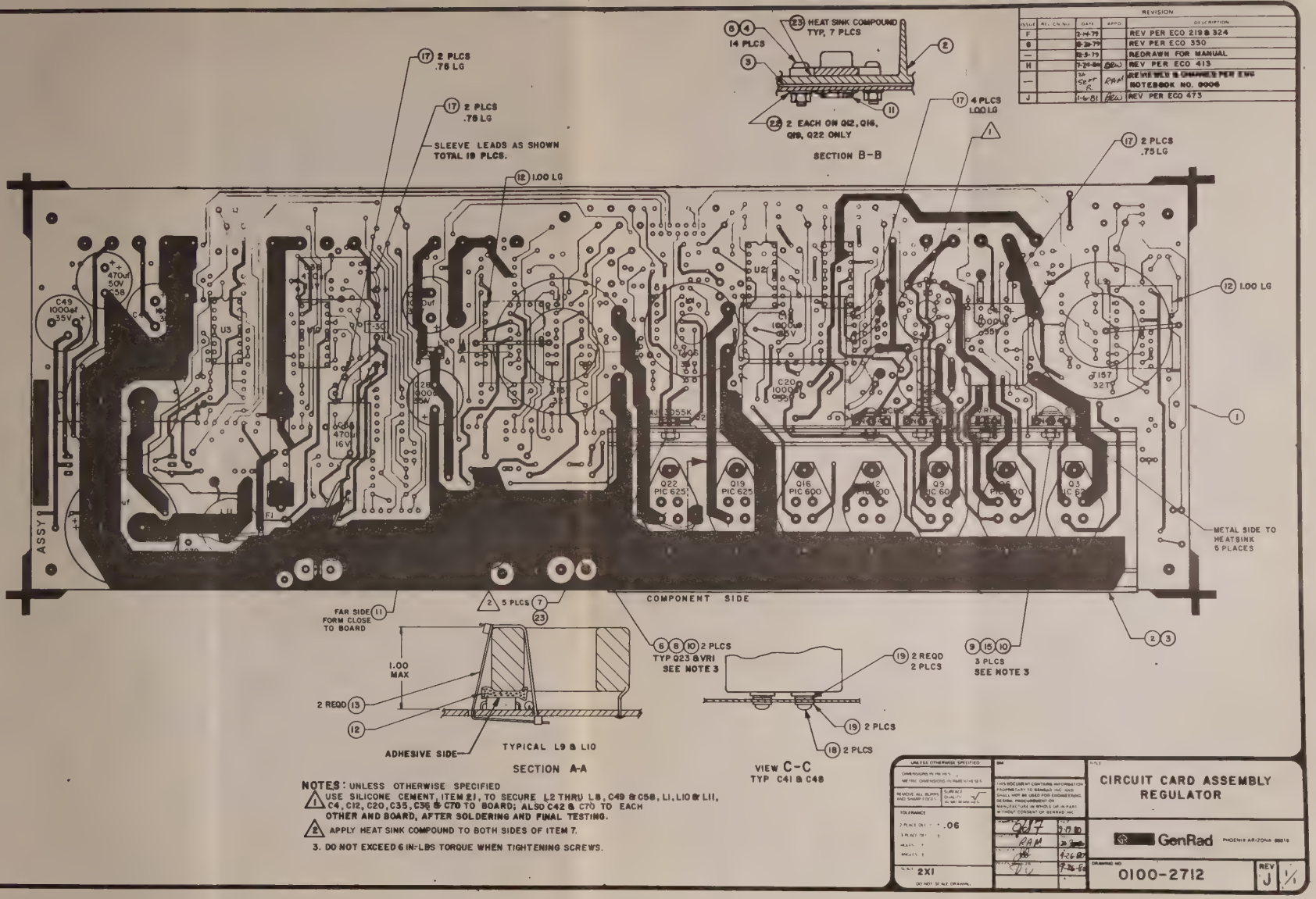
A	9508-38			REL PER 0100-9500-38
–		27 SEP 80	AAM	REVIEWED & CHANGED PER ENG NOTEBOOK NO. 0005
B		16-81	GCW	REV PER ECO 473



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS ±5%, 1/4 W.
2. ALL 1% RESISTORS ARE 1/8 W.
3. THE FOLLOWING MUST BE MOUNTED .120±.03 ABOVE BOARD SURFACE: R1, R23, R39, R60, R90, R105, R126

R.D. Cook	8-17-83	CIRCUIT CARD ASSEMBLY REGULATOR
		GenRad
		0100-1712 REV B


REVISION
ISSUE | REL. ENG. NO. | DATE | APPD. | DESCRIPTION
F | | 2-14-79 | | REV PER ECO 219 & 324
G | | 6-26-79 | | REV PER ECO 350
— | | 12-5-79 | | REDRAWN FOR MANUAL
H | | 7-24-80 | DEW | REV PER ECO 413
— | | 10 SEPT 81 | RAM | REVISED & CHANGED PER ENG NOTEBOOK NO. 9006
J | | 1-6-81 | DEW | REV PER ECO 473
(8)(4) 14 PLCS
(23) HEAT SINK COMPOUND TYP, 7 PLCS
(2)
(3)
(11)
(22) 2 EACH ON Q2, Q16, Q19, Q22 ONLY
SECTION B-B
(17) 2 PLCS .75 LG
(17) 2 PLCS .75 LG
SLEEVE LEADS AS SHOWN TOTAL 19 PLCS.
(12) 1.00 LG
(17) 4 PLCS 1.00 LG
(1)
(17) 2 PLCS .75 LG
(12) 1.00 LG
(1)
METAL SIDE TO HEATSINK 5 PLACES
ASSY 1
C49 1000uf 35V
470uf 50V
C58
C68 470uf 16V
C20 1000uf 35V
Q22 PIC 625
Q19 PIC 625
Q16 PIC 600
Q9 PIC 60
Q3 PIC 60
(2)(3)
COMPONENT SIDE
(2) 5 PLCS (7) (23)
FAR SIDE (11) FORM CLOSE TO BOARD
1.00 MAX
2 REQD (13)
(12)
ADHESIVE SIDE
TYPICAL L9 & L10
SECTION A-A
(6)(8)(10) 2 PLCS TYP Q23 & VR1 SEE NOTE 3
(19) 2 REQD 2 PLCS
(9)(15)(10) 3 PLCS SEE NOTE 3
(19) 2 PLCS
(18) 2 PLCS
VIEW C-C TYP C41 & C48
NOTES: UNLESS OTHERWISE SPECIFIED
(1) USE SILICONE CEMENT, ITEM 21, TO SECURE L2 THRU L8, C49 & C58, L1, L10 & L11, C4, C12, C20, C35, C36 & C70 TO BOARD; ALSO C42 & C70 TO EACH OTHER AND BOARD, AFTER SOLDERING AND FINAL TESTING.
(2) APPLY HEAT SINK COMPOUND TO BOTH SIDES OF ITEM 7.
3. DO NOT EXCEED 6 IN-LBS TORQUE WHEN TIGHTENING SCREWS.
UNLESS OTHERWISE SPECIFIED
TOLERANCE
.06
2XI
DO NOT SCALE DRAWING
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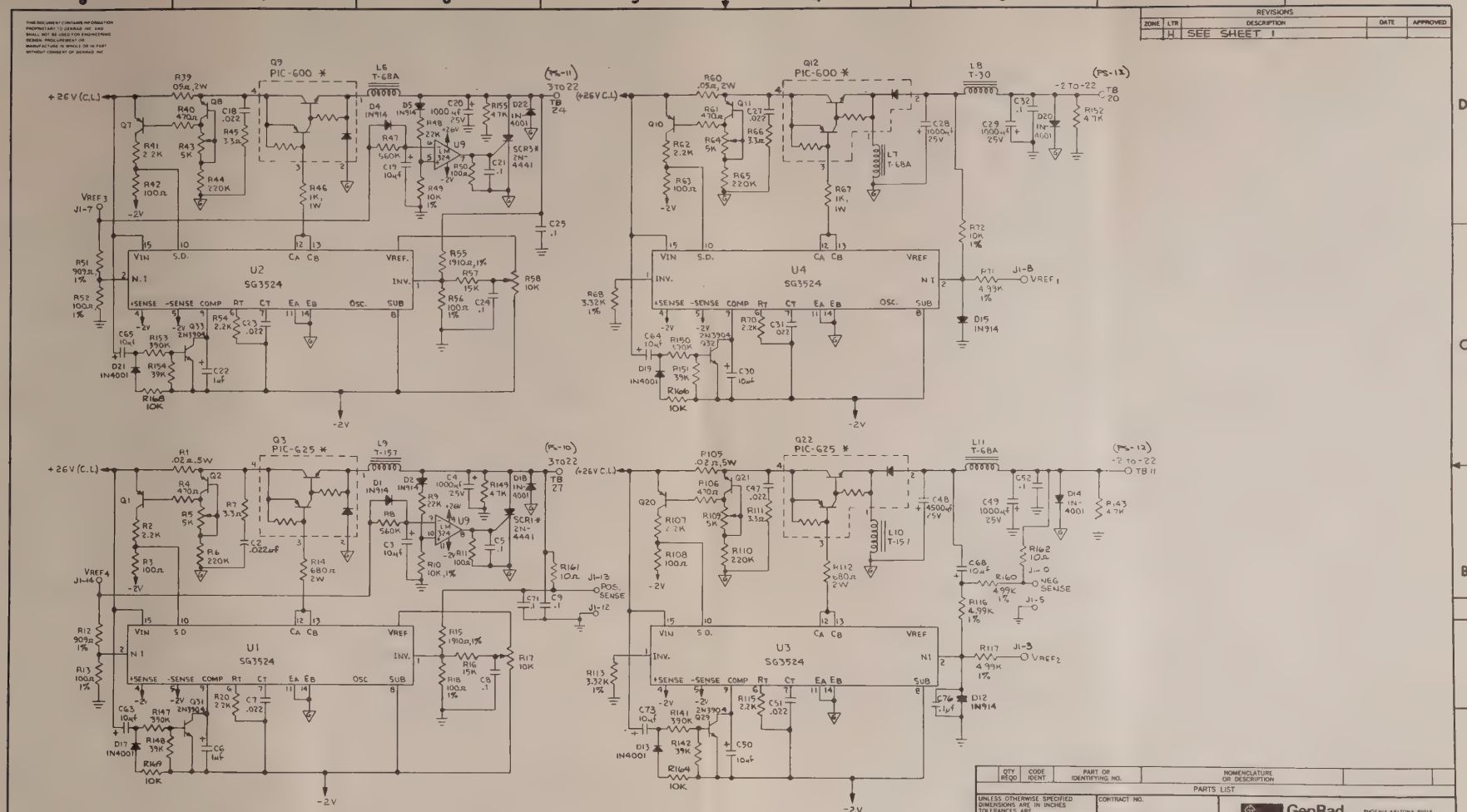
CHK'D
APP'D
MFG
QUAL
CIRCUIT CARD ASSEMBLY REGULATOR
GenRad PHOENIX ARIZONA 85018
DRAWING NO. 0100-2712
REV J
SHEET 1/1



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	H	SEE SHEET 1		

1. ASTERISK (*) INDICATES HEAT-SINK.

NOTES:

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

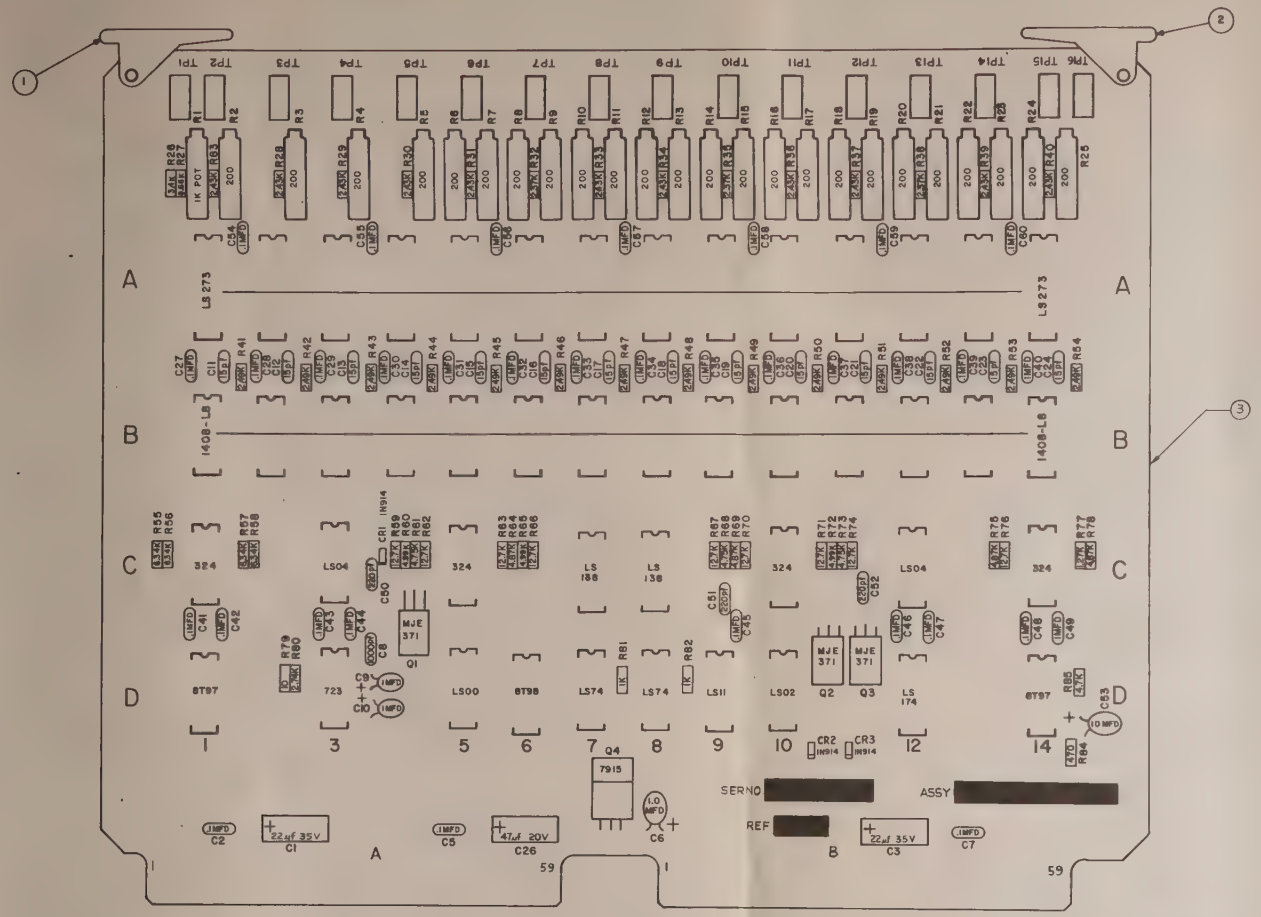
APPROVALS	DATE
DRAWN L. DALES	9-19-80
CHECKED R.A.M.	25 Sep 80
ENGINEERING	9-24-80
APPROVED	9-25-80

GenRad PHOENIX ARIZONA 85016

SCHEMATIC DIAGRAM
REGULATOR

SIZE	CODE IDENT NO	DRAWING NO	REV
D		0100-2712	H

SCALE | SHEET 2 OF 2



REVISION				
ISSUE	REL CN NO	DATE	APPD	DESCRIPTION
F		7-29-79	[illegible]	REDRAWN W/O PHYSICAL CHG ECO 330
G		10-11-79	[illegible]	UPDATED PER ECO 352 & 356
—		12-17-79	[illegible]	REDRAWN WITHOUT CHANGE
H		7-30-80	BDJ	REV PER ECO 447
—		9-25-80	RAM	REVIEWED & CHANGED PER ENG NOTEBOOK NO. 0005

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
METRIC DIMENSIONS IN PARENTHESES
REMOVE ALL BURRS AND SHARP EDGES
SURFACE QUALITY IN MICROINCHES
TOLERANCE
2 PLACE DEC ± .
3 PLACE DEC ± .
HOLES ±
ANGLES ±
SCALE
DO NOT SCALE DRAWING

THIS DOCUMENT CONTAINING INFORMATION PROPRIETARY TO GENRAD, INC. AND SHALL NOT BE USED FOR ENGINEERING DESIGN, PROCUREMENT OR MANUFACTURING PURPOSES EXCEPT PURSUANT TO WRITTEN AGREEMENT WITH GENRAD, INC.

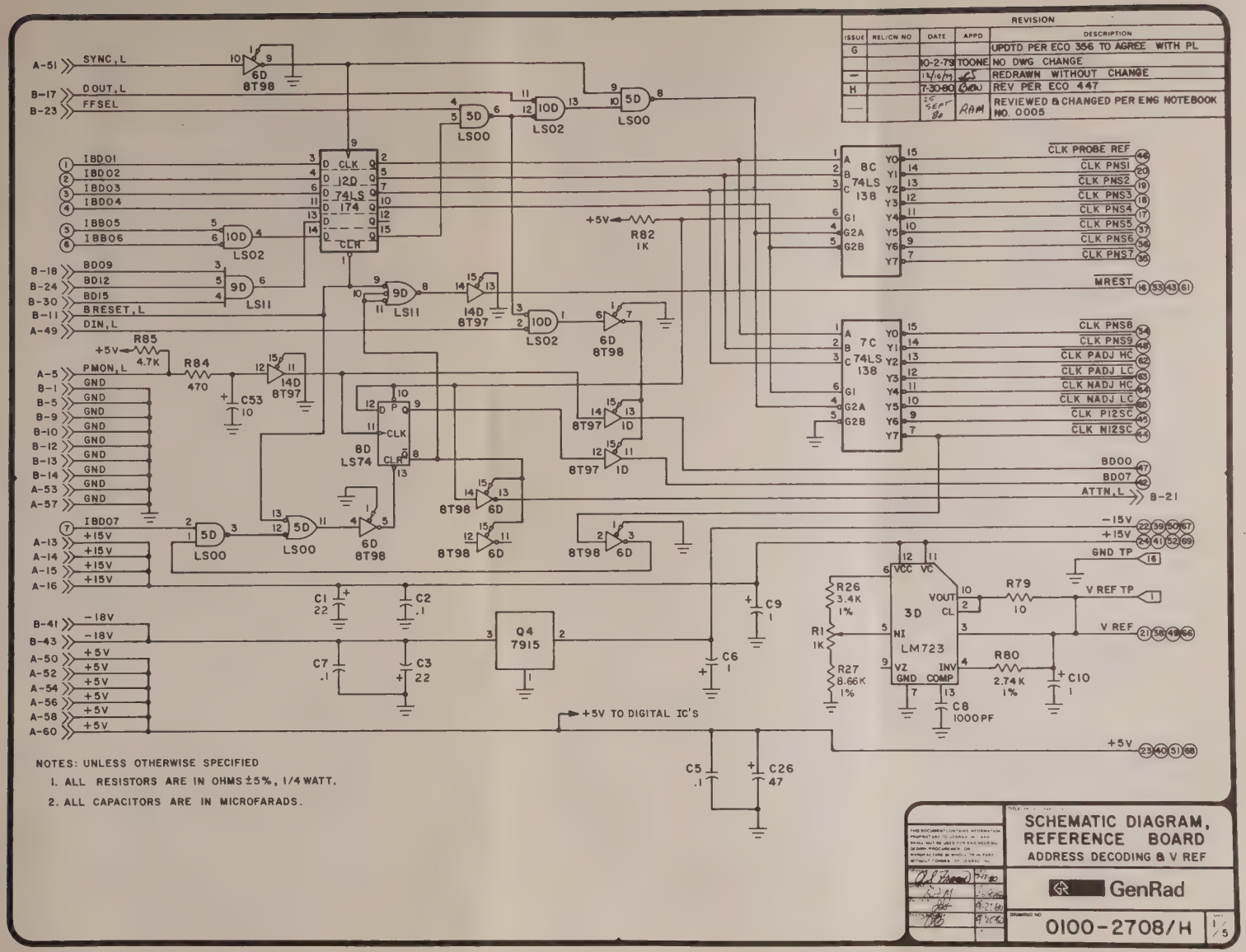
DRAWN [signature] 9-17-80
CHECKED RAM 9-25-80
ENGR [signature] 9-25-80
MFG ENGR [signature] 9-25-80

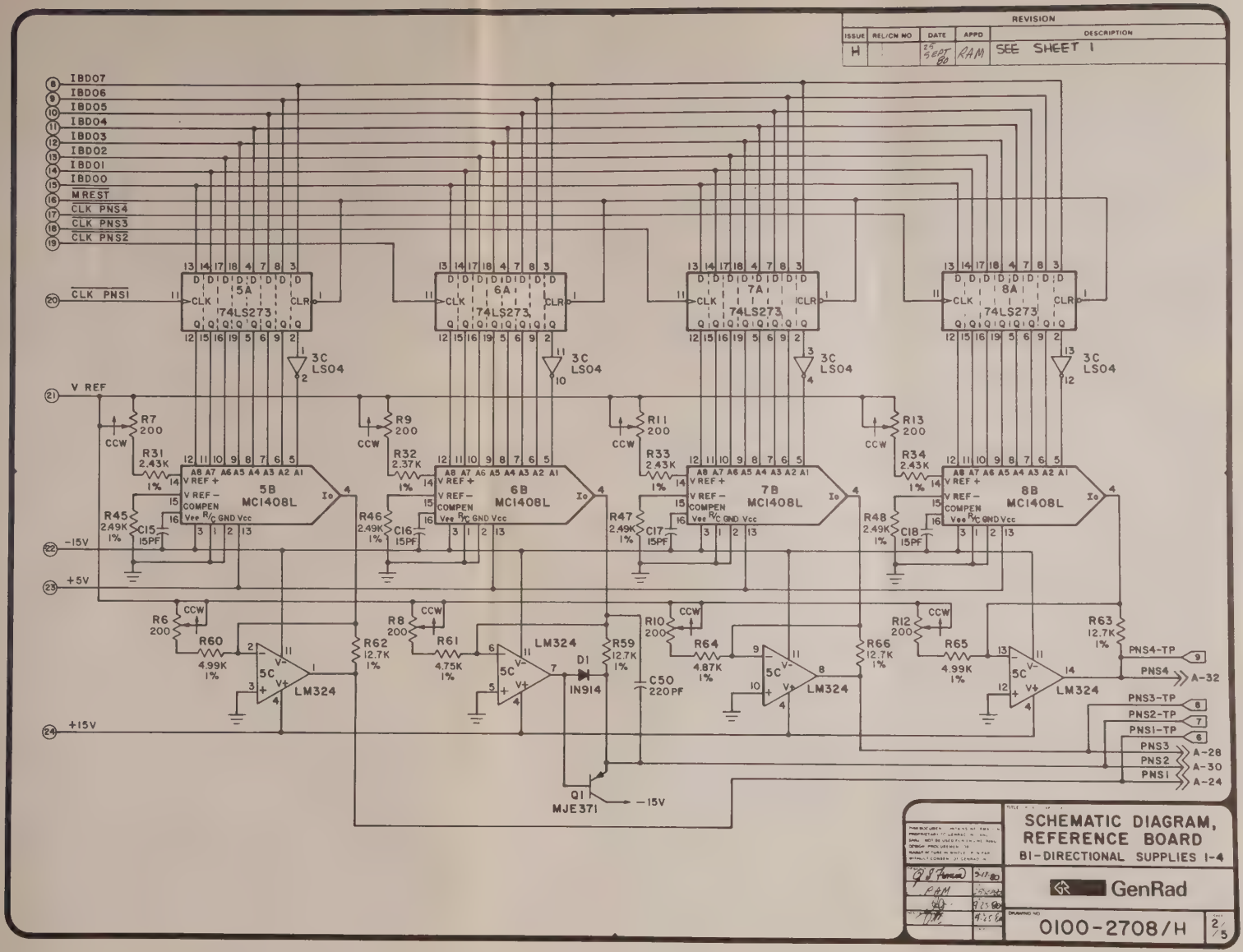
CIRCUIT CARD ASSEMBLY REFERENCE

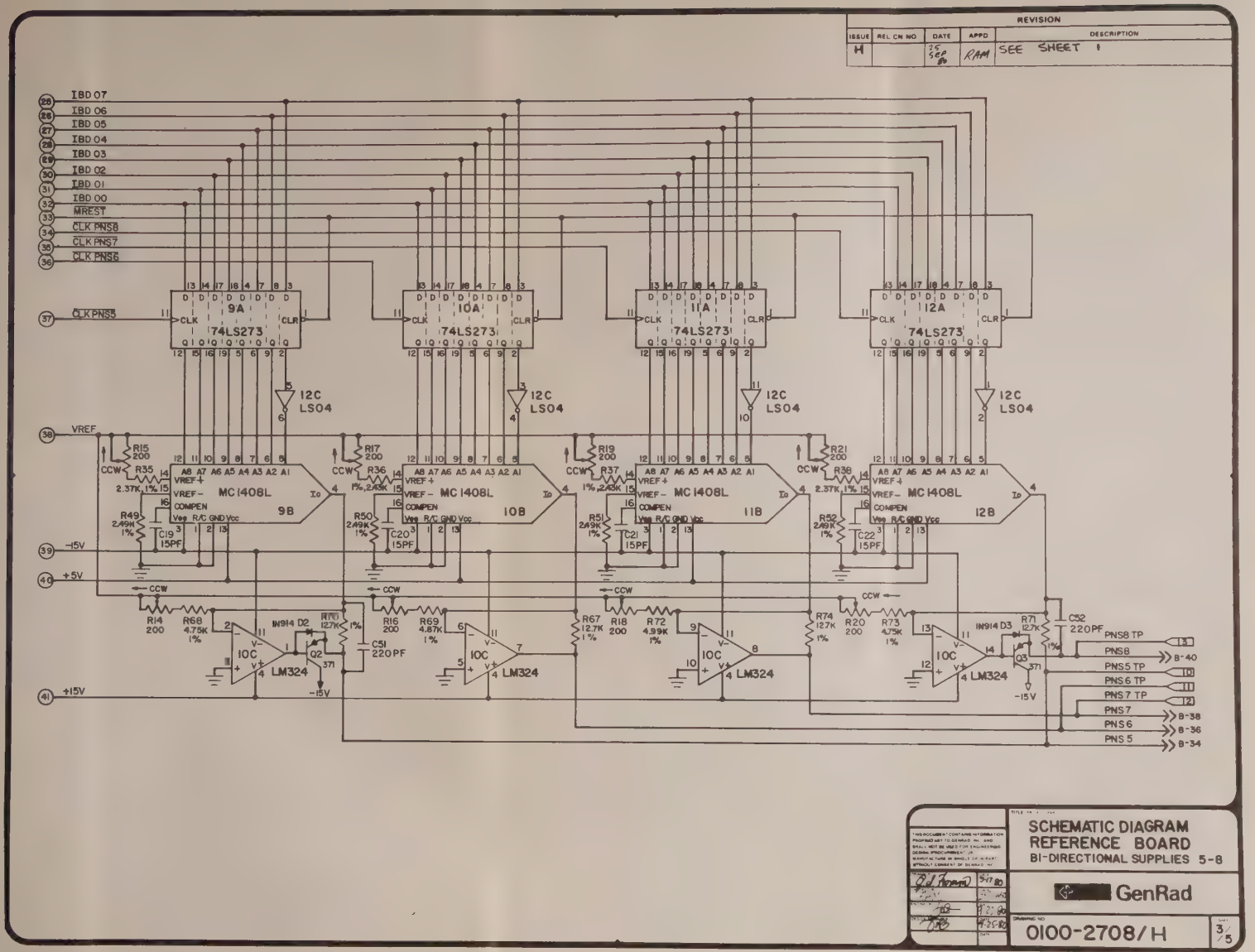
GenRad

0100-2708/H

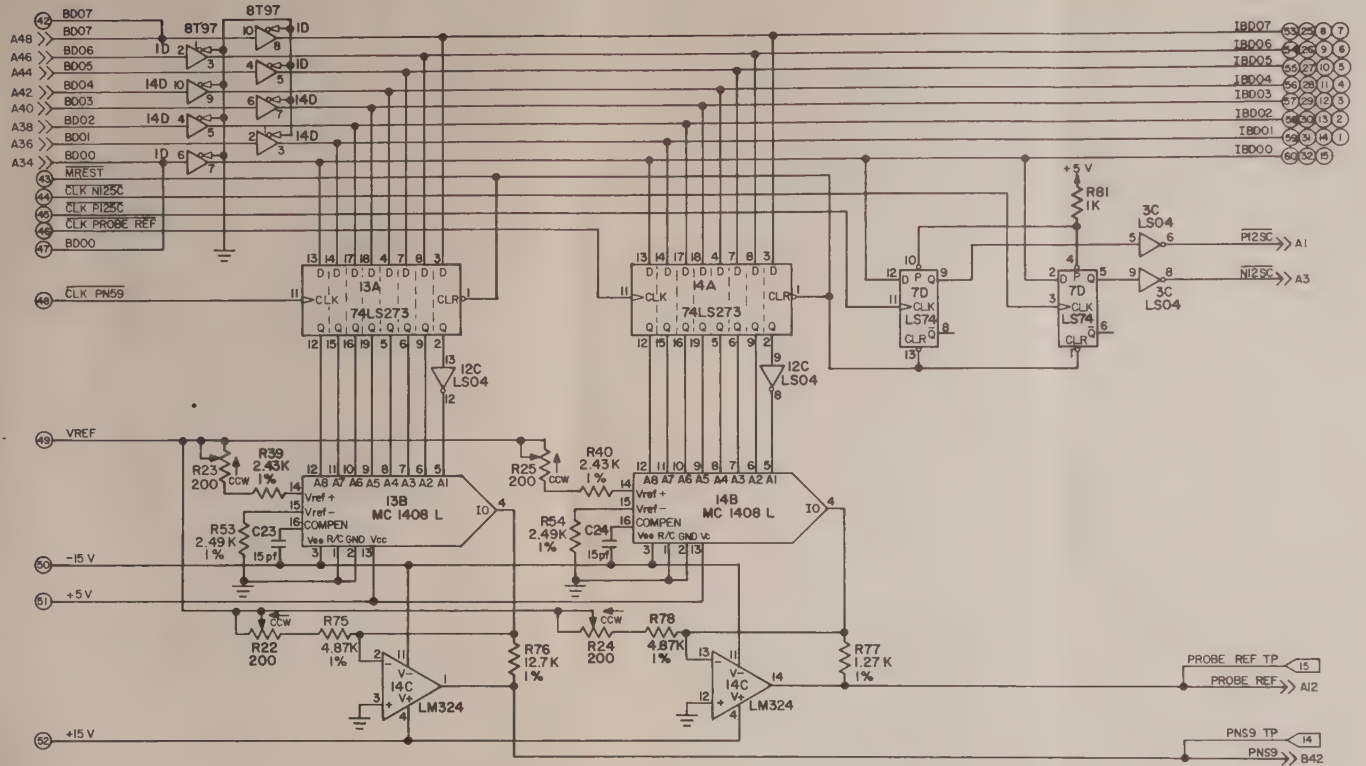
SHEET 1/1


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
G | | | | UPDTD PER ECO 356 TO AGREE WITH PL
| | 10-2-79 | TOONE | NO DWG CHANGE
— | | 11/6/79 | | REDRAWN WITHOUT CHANGE
H | | 7-30-80 | | REV PER ECO 447
| | 25 SEPT 80 | RAM | REVIEWED & CHANGED PER ENG NOTEBOOK NO. 0005
A-51 SYNC,L
B-17 DOUT,L
B-23 FFSEL
IBD01
IBD02
IBD03
IBD04
IBB05
IBB06
B-18 BD09
B-24 BD12
B-30 BD15
B-11 BRESET,L
A-49 DIN,L
A-5 PMON,L
B-1 GND
B-5 GND
B-9 GND
B-10 GND
B-12 GND
B-13 GND
B-14 GND
A-53 GND
A-57 GND
IBD07
A-13 +15V
A-14 +15V
A-15 +15V
A-16 +15V
B-41 -18V
B-43 -18V
A-50 +5V
A-52 +5V
A-54 +5V
A-56 +5V
A-58 +5V
A-60 +5V
+5V TO DIGITAL IC'S
CLK PROBE REF
CLK PNS1
CLK PNS2
CLK PNS3
CLK PNS4
CLK PNS5
CLK PNS6
CLK PNS7
MREST
CLK PNS8
CLK PNS9
CLK PADJ HC
CLK PADJ LC
CLK NADJ HC
CLK NADJ LC
CLK PI2SC
CLK NI2SC
BD00
BD07
ATTN,L
B-21
-15V
+15V
GND TP
V REF TP
V REF
+5V
R85 4.7K
R84 470
C53 10
R82 1K
C1 22
C2 .1
C7 .1
C3 22
Q4 7915
C9 1
C6 1
R26 3.4K 1%
R1 1K
R27 8.66K 1%
R79 10
R80 2.74K 1%
C10 1
C8 1000PF
C5 .1
C26 47
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS ±5%, 1/4 WATT.
2. ALL CAPACITORS ARE IN MICROFARADS.
SCHEMATIC DIAGRAM, REFERENCE BOARD
ADDRESS DECODING & V REF
GenRad
0100-2708/H
1/5


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
H | | 25 SEPT 80 | RAM | SEE SHEET 1
IBD07
IBD06
IBD05
IBD04
IBD03
IBD02
IBD01
IBD00
MREST
CLK PNS4
CLK PNS3
CLK PNS2
CLK PNS1
5A 74LS273
6A 74LS273
7A 74LS273
8A 74LS273
3C LS04
V REF
R7 200
R9 200
R11 200
R13 200
R31 2.43K 1%
R32 2.37K 1%
R33 2.43K 1%
R34 2.43K 1%
5B MC1408L
6B MC1408L
7B MC1408L
8B MC1408L
R45 2.49K 1%
R46 2.49K 1%
R47 2.49K 1%
R48 2.49K 1%
C15 15PF
C16 15PF
C17 15PF
C18 15PF
-15V
+5V
+15V
R6 200
R8 200
R10 200
R12 200
R60 4.99K 1%
R61 4.75K 1%
R64 4.87K 1%
R65 4.99K 1%
R62 12.7K 1%
R59 12.7K 1%
R66 12.7K 1%
R63 12.7K 1%
5C LM324
D1 IN914
C50 220PF
Q1 MJE371
PNS4-TP
PNS4
PNS3-TP
PNS2-TP
PNS1-TP
PNS3
PNS2
PNS1
A-32
A-28
A-30
A-24
SCHEMATIC DIAGRAM, REFERENCE BOARD
BI-DIRECTIONAL SUPPLIES 1-4
GenRad
0100-2708/H
2/5


REVISION
ISSUE | REL CN NO | DATE | APPD | DESCRIPTION
H | | 22 SEP 80 | RAM | SEE SHEET 1
IBD 07
IBD 06
IBD 05
IBD 04
IBD 03
IBD 02
IBD 01
IBD 00
MREST
CLK PNS8
CLK PNS7
CLK PNS6
CLK PNS5
VREF
-15V
+5V
+15V
9A
10A
11A
12A
74LS273
12C LS04
9B
10B
11B
12B
MC1408L
R15 200
R17 200
R19 200
R21 200
R35 2.37K 1%
R36 2.43K 1%
R37 2.43K 1%
R49 2.49K 1%
R50 2.49K 1%
R51 2.49K 1%
R52 2.49K 1%
C19 15PF
C20 15PF
C21 15PF
C22 15PF
CCW
R14 200
R68 4.75K 1%
R16 200
R69 4.87K 1%
R67 12.7K 1%
R18 200
R72 4.99K 1%
R74 12.7K 1%
R20 200
R73 4.75K 1%
R70 127K 1%
R71 127K 1%
C51 220PF
C52 220PF
IN914 D2
IN914 D3
Q2
Q3
10C
LM324
PNS8 TP
PNS8
PNS5 TP
PNS6 TP
PNS7 TP
PNS7
PNS6
PNS5
B-40
B-38
B-36
B-34
SCHEMATIC DIAGRAM
REFERENCE BOARD
BI-DIRECTIONAL SUPPLIES 5-8
GenRad
0100-2708/H
3/5

REVISION				
ISSUE	REL/CN NO	DATE	APPD	DESCRIPTION
H		25 SEP 80	RAM	SEE SHEET 1



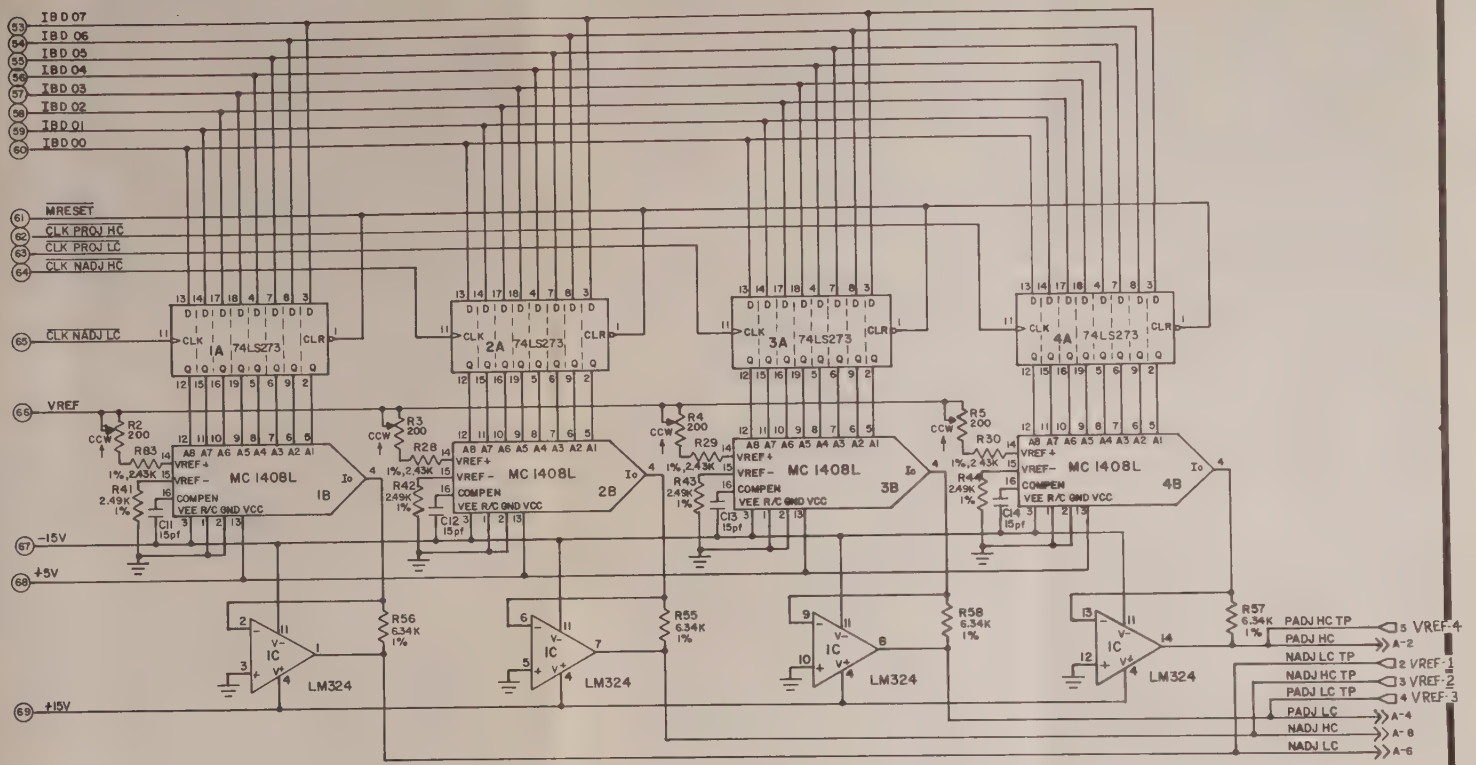
SCHEMATIC DIAGRAM, REFERENCE BD
BI-DIRECTIONAL SUPPLY & PROBE REFERENCE, +12V & -12V BUT SUPPLY

GenRad

0100-2708/H

4/5

REVISION				
ISSUE	REL/CN NO	DATE	APPD	DESCRIPTION
H		25 SEP 80	RAM	SEE SHEET 1



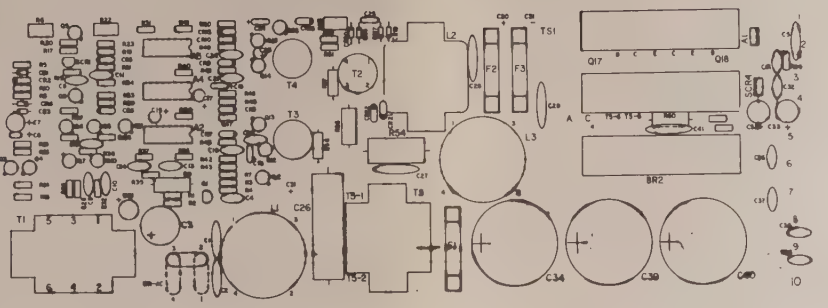
SCHEMATIC DIAGRAM
REFERENCE BD
UNI-DIRECTIONAL SUPPLIES

GenRad

0100-2708 / H

5/5

REVISIONS				
REV	ZONE	DESCRIPTION	DATE	APPROVED
D		REV UPDATE TO MATCH PRODUCTION 11273		
D1		ECO 1558 C1/C2 WERE .01uF, 1.4KV	8-9-78	



MATERIAL: .062 THICK FR4 GLASS FILLED EPOXY 1 OZ. COPPER MIN. BOTH SIDES (OR EQUIVALENT)

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INTERPRET DIM AND TOL PER USAS Y14.5

UNLESS OTHERWISE SPECIFIED, DIM ARE IN INCHES.

TOLERANCE 2 PL DEC ± 3 PL DEC ±

ANGLES ±

DRAWN BY DATE

CHECKED BY DATE

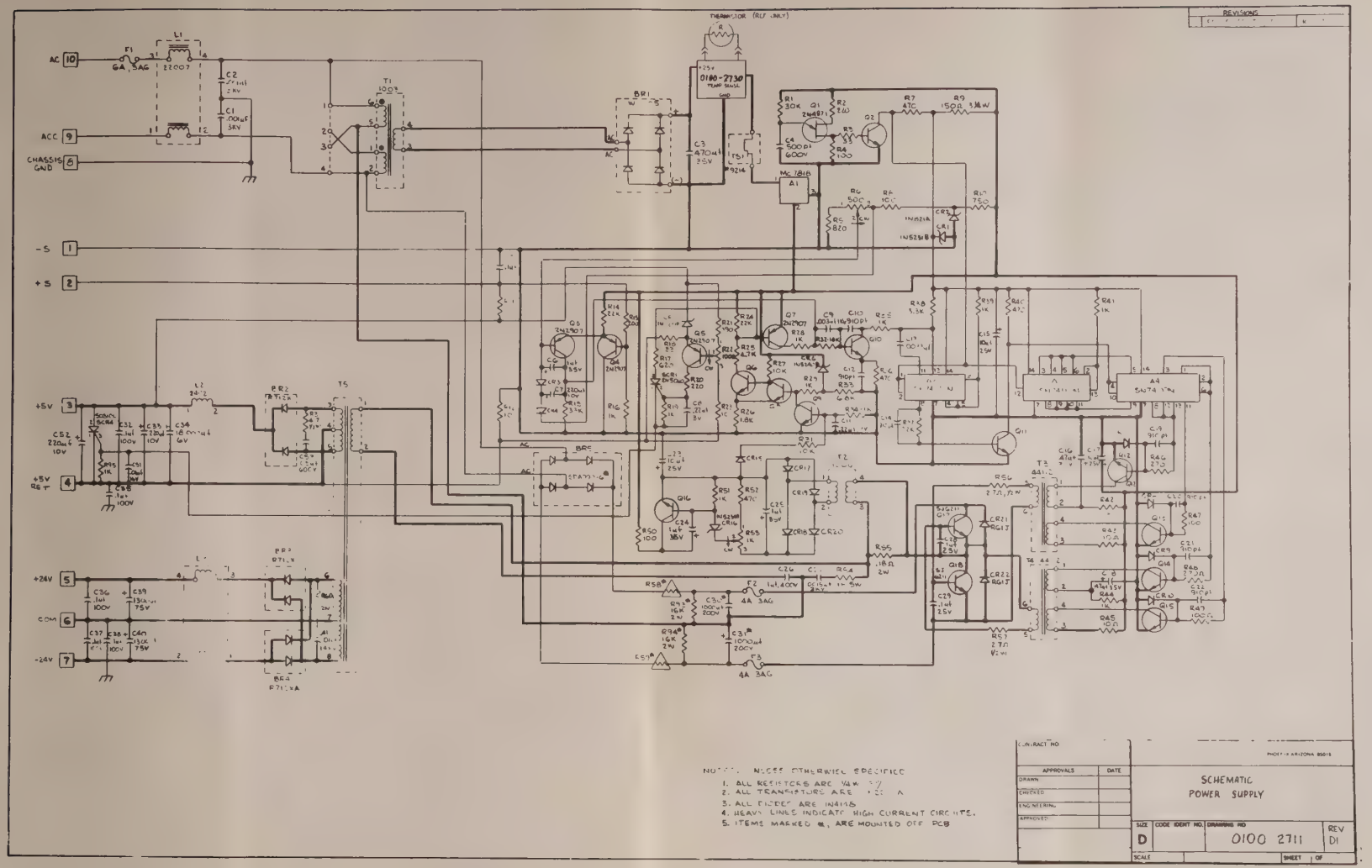
APPROVED BY DATE

PHOENIX, ARIZONA

TITLE PCB ASSY POWER SUPPLY

SIZE C | DRAWING NO. 0100-2711 | REV D1

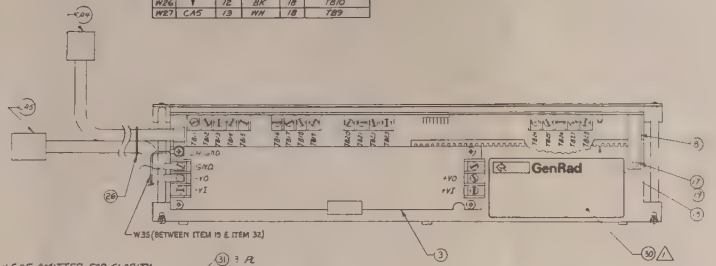
SCALE 1/1 SHEET OF


REVISIONS
AC 10
ACC 9
CHASSIS GND 8
-S 1
+S 2
+5V 3
+5V REF 4
+24V 5
COM 6
-24V 7
F1 6A, 3AG
L1 22007
T1 1009
BR1
THERMISTOR (RLF ONLY)
0180-2730
MC 7818
A1
A2 SN74 LS74N
A3 SN74 LS74N
A4 SN74 LS74N
F2 4A 3AG
F3 4A 3AG
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W ±5%
2. ALL TRANSISTORS ARE 2N3904
3. ALL DIODES ARE 1N4148
4. HEAVY LINES INDICATE HIGH CURRENT CIRCUITS.
5. ITEMS MARKED ⊗, ARE MOUNTED OFF PCB
CONTRACT NO.
APPROVALS
DRAWN
CHECKED
ENGINEERING
APPROVED
DATE
PHOENIX ARIZONA 85015
SCHEMATIC
POWER SUPPLY
SIZE D
CODE IDENT NO.
DRAWING NO 0100 2711
REV D1
SCALE
SHEET OF

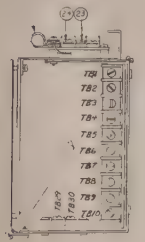
CABLE WIRING LIST					
WIRE NO.	TERMINATION CABLE NO.	TERMINATION PIN NO.	WIRE COLOR	WIRE AWG	TERMINATION TERM NO.
W1	CA4	1	BU/VT	16	TB11
W2		2	BU/VT	16	TB11
W3		3	WH/GN	20	TB13
W4		4	WH/OR	18	TB15
W5		5	BK	16	TB21
W6		6	OR	20	TB26
W7		7	BU/OR	18	TB19
W8		8	BU/GN	18	TB20
W9		9	GY/OR	18	TB23
W10		10	BK	16	TB21
W11		11	BU	20	+V0
W12		12	GY/GN	18	TB24
W13		13	YL	20	TB25
W14		14	GY/VT	16	TB27
W15	CA4	15	GY/VT	16	TB27
W16	CA5	1	BK	20	TB30
W17		2	BK	24	TB1
W18		3	RD	24	TB2
W19		4	WH/BU	20	-V0
W20		5	RD	16	TB3
W21		6	RD	16	TB3
W22		8	BK	16	TB4
W23		9	BK	16	TB4
W24		10	GN/YL	18	TB8
W25		11	BN	20	TB29
W26		12	BK	18	TB10
W27	CA5	13	WH	18	TB9

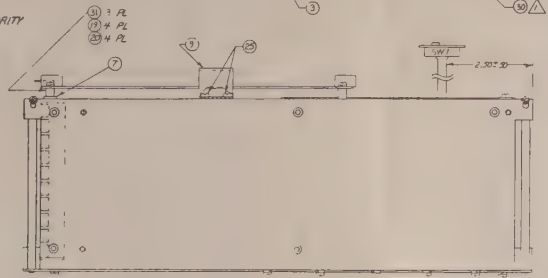
INTERNAL WIRE LIST								
WIRE NO.	FROM TERM NO.	TERM TYPE	WIRE ITEM	WIRE COLOR	WIRE AWG	WIRE CUT LENGTH	TO TERM TYPE	TO TERM NO.
W28	TB16	IT-16	10	VT	16	10 IN	IT-16	TB5
W29	TB15	IT-16	11	BK	16	10 IN.	IT-16	TB6
W30	TB22	IT-29	12	BK	14	12 IN.	IT-29	TB6
W31	TB14	IT-16	13	BK	18	6 IN.	IT-16	GND
W32	TB17	IT-16	14	VT	18	9 IN.	IT-16	+V1
W33	TB18	IT-16	19	VT	18	10 IN.	IT-16	TB28
W34	TB7	IT-16	27	WH/VT	18	6 IN	IT-16	-V1
W35	TB8	IT-16	28	GN/YL	18	8 IN.	IT-16	CH GND

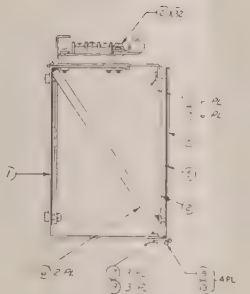
REVISION				
REV	SEE ECN NO.	DATE	APPD	DESCRIPTION
1		4-6-84	JM	ADDED -33 PL
2		9-7-90		LABEL ADDED, WIRE LISTS UPDATED
3		12-6-94	JM	REVISED 1 CHANGE PER ENG NOTEBOOK NO. 9005



(32) CA4 & CA5 OMITTED FOR CLARITY







⚠ MARK ITEM 30 AS FOLLOWS:
ASSY 0123-9000/ ☐ SN
LN 6000-0003/ ☐ SN
24V REG 0100-2713/ ☐ SN
REG 0100-2712/ ☐ SN

NOTES:

0123-9000	323-9805	
VTT 2014	SCD 274	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
METRIC DIMENSIONS IN PARENTHESES
REMOVE ALL BURRS AND SHARP EDGES
SURFACE FINISH 125 MICROINCHES
TOLERANCES
2 PLACE DEC ± .X
3 PLACE DEC ± .XX
ANGLES ±
S.M.I.
FULL
DO NOT SCALE DRAWING
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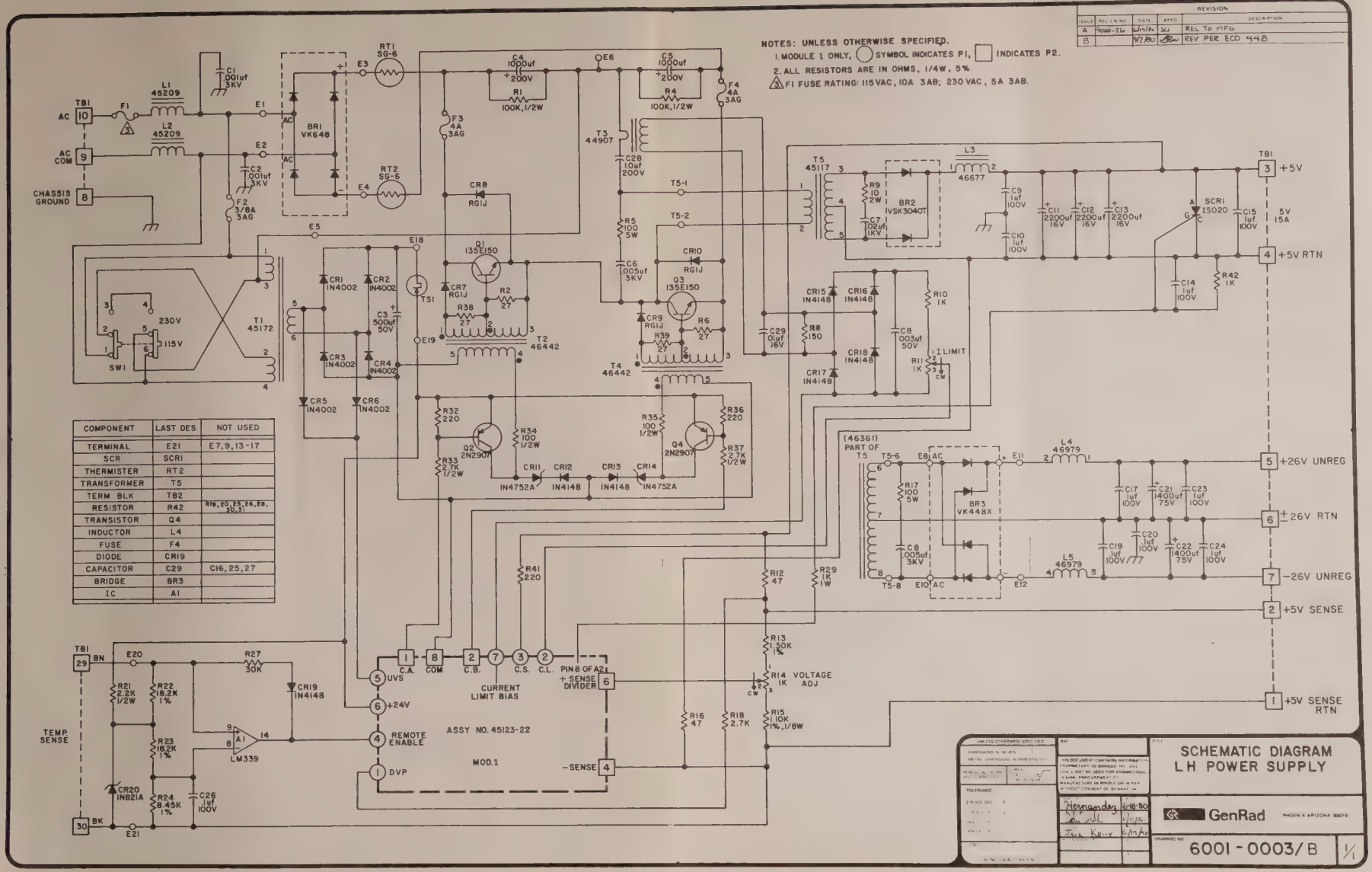
DRAWN J.FROMM 1-9-84
CHECKED 1-12-84
ENGINEER 1-12-84
MFG
QUALITY
APPROVED

TITLE: -33V POWER SUPPLY, PSP
GenRad
DRAWING NO. 0123-3000 1A
SHEET 1/1

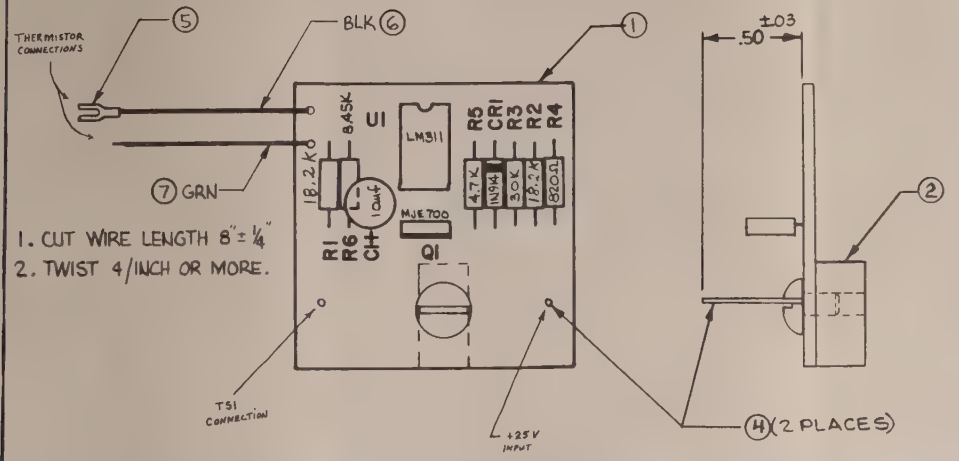


COMPONENT	LAST DES	NOT USED
TERMINAL	E21	E7,9,13-17
SCR	SCR1	
THERMISTER	RT2	
TRANSFORMER	T5	
TERM BLK	TB2	
RESISTOR	R42	R18,20,25,26,28, 30,31
TRANSISTOR	Q4	
INDUCTOR	L4	
FUSE	F4	
DIODE	CR19	
CAPACITOR	C29	C16,25,27
BRIDGE	BR3	
IC	A1	

SCHEMATIC DIAGRAM
LH POWER SUPPLY

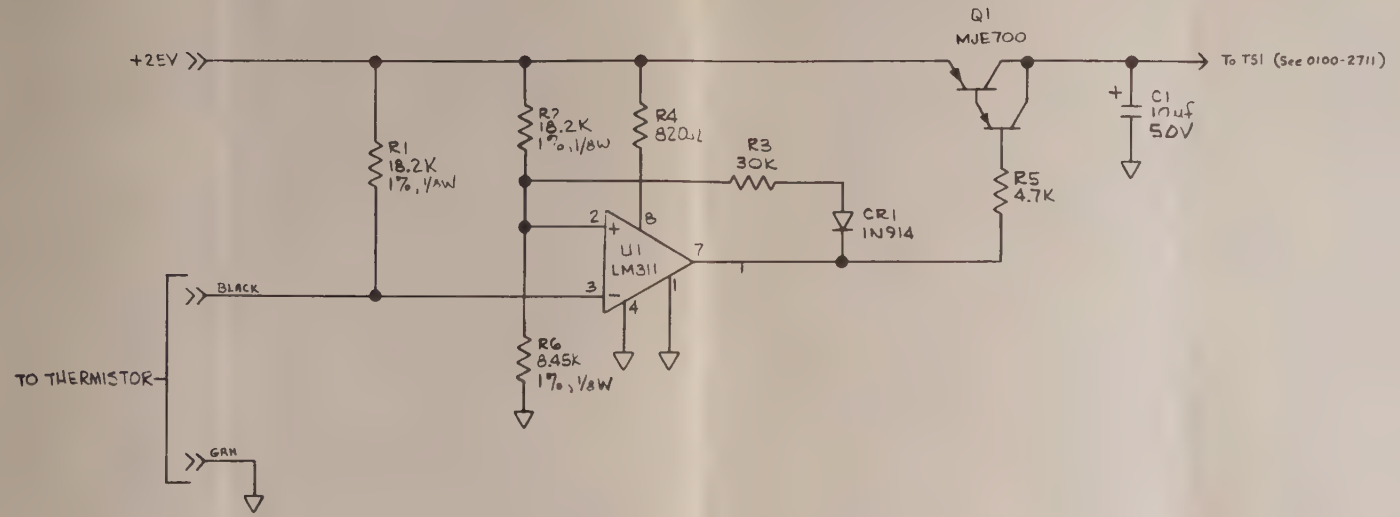
GenRad PHOENIX, ARIZONA 85018

6001-0003/B 1/1



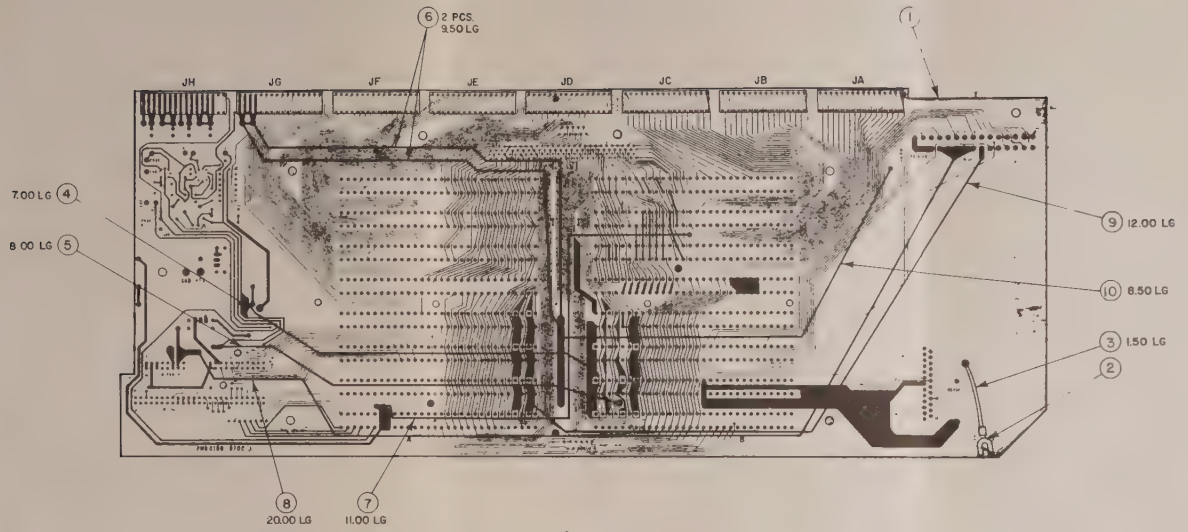
CONTRACT NO.		PHOENIX ARIZONA 85016			
APPROVALS	DATE	ASSY - TEMPERATURE SENSE			
DRAWN L.C. Adams	12/21/77				
CHECKED					
ENGINEERING					
APPROVED					
		SIZE: B	CODE IDENT NO.	DRAWING NO.: 0100-2730	REV.: A2
		SCALE		SHEET 1 OF 1	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
–	B	VOLTAGE OF C1 WAS 35V. ECO 204	1/18/79	J. Sobel



CONTRACT NO.		PHOENIX ARIZONA 85016			
APPROVALS	DATE	SCHEMATIC, TEMPERATURE SENSE			
DRAWN L.C. Davis	12/27/77				
CHECKED					
ENGINEERING					
APPROVED					
		SIZE: B	CODE IDENT NO.	DRAWING NO.: 0100-2730	REV: B
		SCALE: —		SHEET 1 OF	

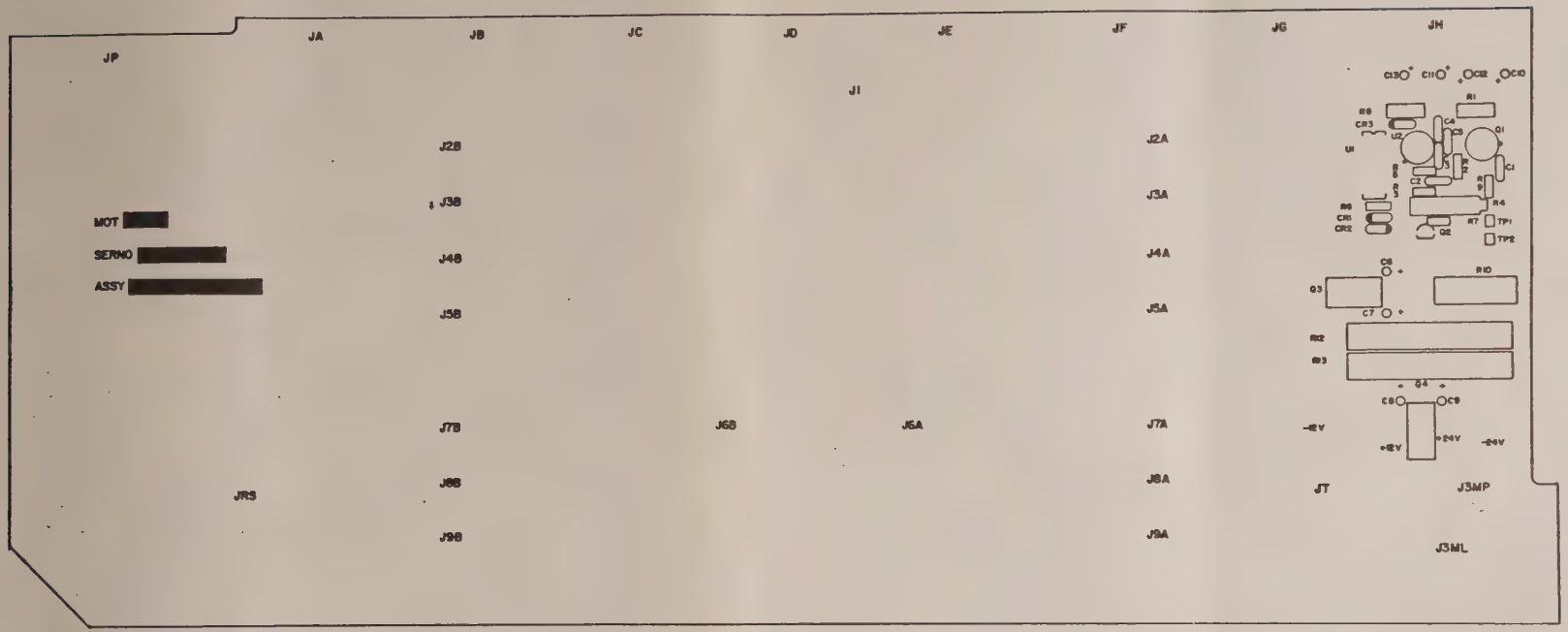
REVISIONS				
ISSUE	REL/CH NO	DATE	APPD	DESCRIPTION
J		11-10-80	RAM	REVISED & REDRAWN PER ENG NTBK NO. 0005



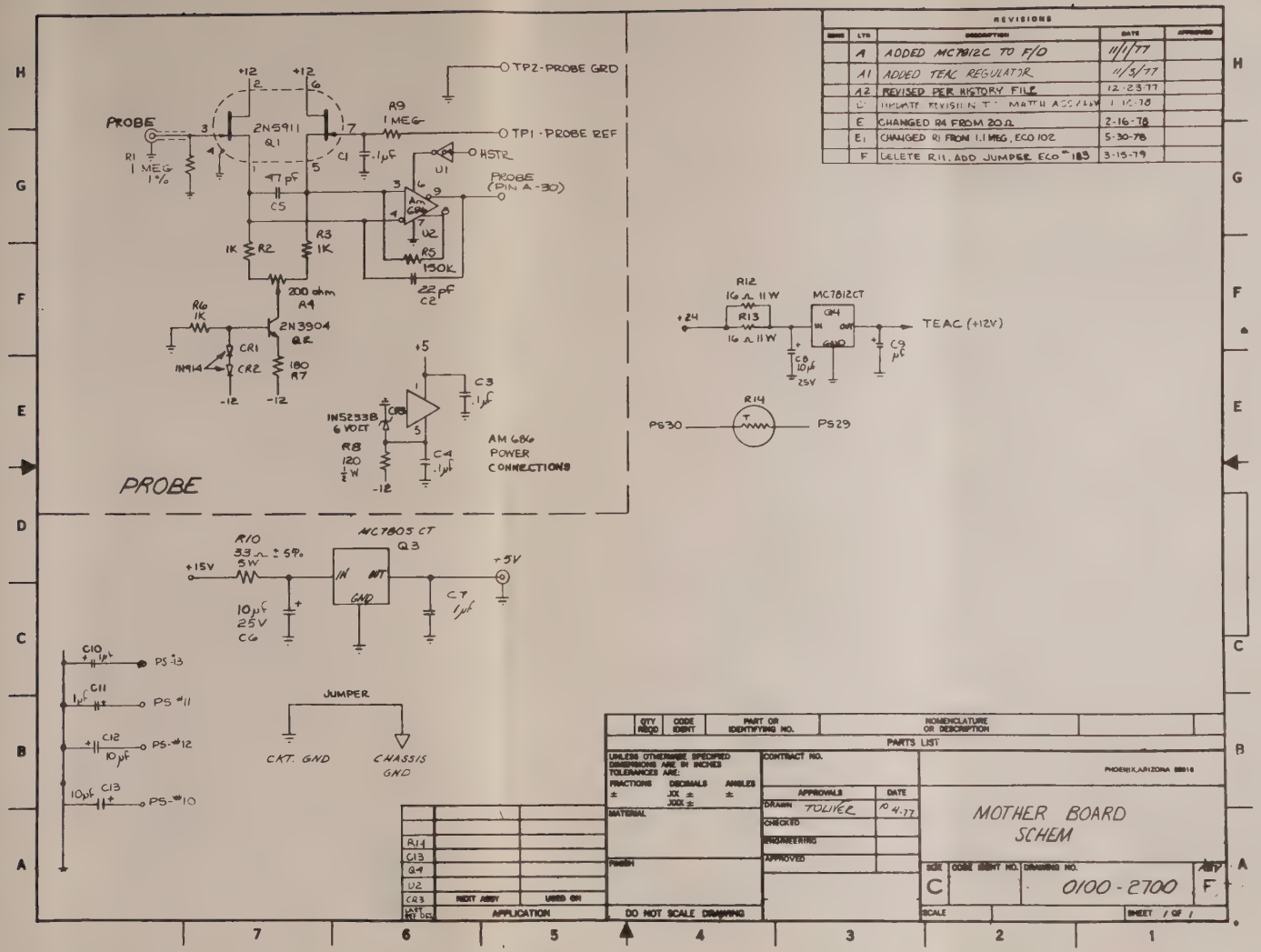
NOTES:

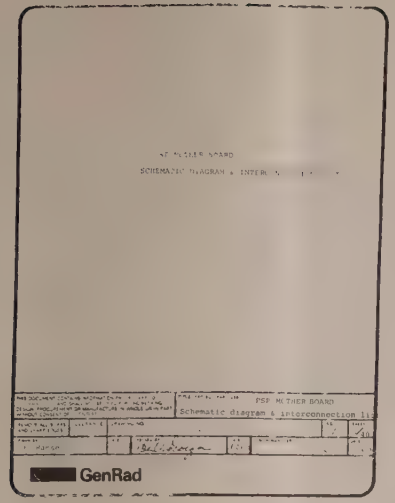
1. STRIP & TIN ALL WIRES .12 EACH.
2. FLUSH CUT PINS ON CONNECTORS JA THRU JH.
3. CUT LEADS OF U2 & Q1 TO .15 AND INSTALL.

UNLESS OTHERWISE SPECIFIED	TITLE PROJECT PART NO.
DIMENSIONS IN INCHES	CIRCUIT CARD ASSY. MOTHER BOARD
METRIC DIMENSIONS IN PARENTHESES	
REMOVE ALL BURRS AND SHARP EDGES	SURFACE QUALITY IN MICROINCHES √
TOLERANCES: 2 PLACE DEC ± .12 3 PLACE DEC ±	
ANGLES ±	
SCALE 1/1 DO NOT SCALE DRAWING	0100-2700 J



0100-0700 Mother Board Connector Identification

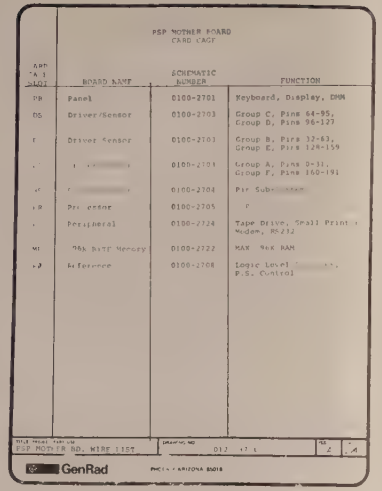

REVISIONS
A ADDED MC7812C TO F/O 11/1/77
A1 ADDED TEAC REGULATOR 11/3/77
A2 REVISED PER HISTORY FILE 12-23-77
E UPDATE REVISION TO MATCH ASSY REV 1-16-78
E1 CHANGED R4 FROM 20Ω 2-16-78
F CHANGED R1 FROM 1.1 MEG, ECO 102 5-30-78
F1 DELETE R11, ADD JUMPER ECO #183 3-15-79
PROBE
TP2-PROBE GRD
TP1-PROBE REF
HSTR
PROBE (PIN A-30)
2N5911 Q1
2N3904 Q2
1N914 CR1 CR2
1N5233B 6 VOLT CR3
AM 686 POWER CONNECTIONS
MC7812CT
MC7805 CT Q3
TEAC (+12V)
+15V
+5V
JUMPER
EXT. GND
CHASSIS GND
PS #13
PS #11
PS #12
PS #10
PS30
PS29
PARTS LIST
CONTRACT NO.
DRAWN TOLIVER 10 4.77
MOTHER BOARD SCHEM
SIZE C
DRAWING NO. 0100-2700
REV F
SCALE
SHEET 1 OF 1
DO NOT SCALE DRAWING



PSP MOTHER BOARD

Schematic diagram & interconnection li

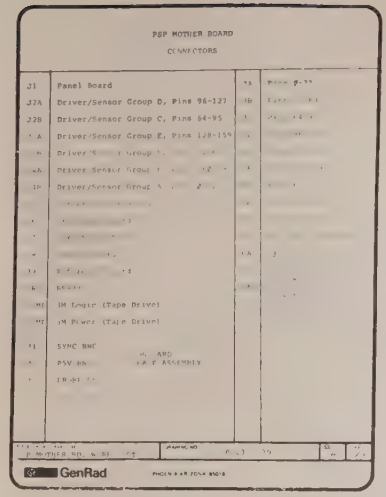
GenRad



PSP MOTHER BOARD
CARD CAGE

ARP CAGE SLOT	BOARD NAME	SCHEMATIC NUMBER	FUNCTION
P8	Panel	0100-2701	Keyboard, Display, DMM
D5	Driver/Sensor	0100-2703	Group C, Pins 64-95, Group D, Pins 96-127
[illegible]	Driver Sensor	0100-2703	Group B, Pins 32-63, Group E, Pins 128-159
[illegible]	[illegible]	0100-2703	Group A, Pins 0-31, Group F, Pins 160-191
[illegible]	[illegible]	0100-2704	Pin Sub- [illegible]
[illegible]R	Pr[illegible]cessor	0100-2705	P
[illegible]	Peripheral	0100-2724	Tape Drive, Small Printer, Modem, RS-232
M[illegible]	96k BATT Memory	0100-2722	MAX 96K RAM
[illegible]8	Reference	0100-2708	Logic Level [illegible], P.S. Control

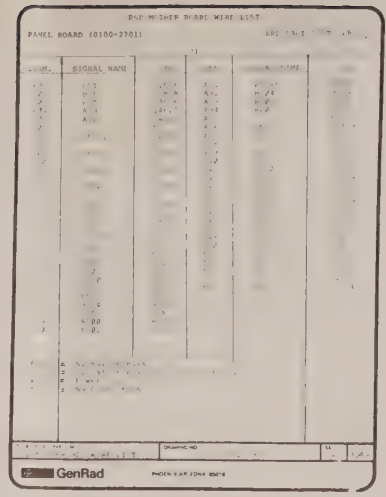
PSP MOTHER BD. WIRE LIST | DRAWING NO 0123-[illegible] | GenRad | PHOENIX ARIZONA 85018



PSP MOTHER BOARD
CONNECTORS

J1	Panel Board	J5	Power [illegible]
J2A	Driver/Sensor Group D, Pins 96-127	J3B	Fan [illegible]
J2B	Driver/Sensor Group C, Pins 64-95	J3	[illegible]
J3A	Driver/Sensor Group E, Pins 128-159	J4	[illegible]
J3	Driver/Sensor Group [illegible]	J5	[illegible]
J3A	Driver Sensor Group [illegible]	J6	[illegible]
J3	Driver/Sensor Group [illegible]	J7	[illegible]
J4	[illegible]	J8	[illegible]
J5	[illegible]	J9	[illegible]
J6	[illegible]	J10	[illegible]
J7	[illegible]	J11	[illegible]
J8	[illegible]	J12	[illegible]
J9	IM Logic (Tape Drive)	J13	[illegible]
J10	IM Power (Tape Drive)	J14	[illegible]
J11	SYNC BNC	J15	[illegible]
J12	PSV BD [illegible]	J16	[illegible]
J13	[illegible]	J17	[illegible]

P. MOTHER BD. WIRE [illegible] | DRAWING NO [illegible] | GenRad | PHOENIX ARIZONA 85018

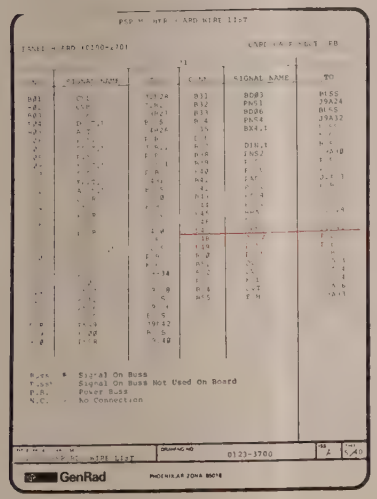


PSP MOTHER BOARD WIRE LIST

PANEL BOARD (0100-2701)

J1 PIN	SIGNAL NAME	J2A PIN	J2B PIN
[illegible]	[illegible]	[illegible]	[illegible]

GenRad | PHOENIX ARIZONA 85018



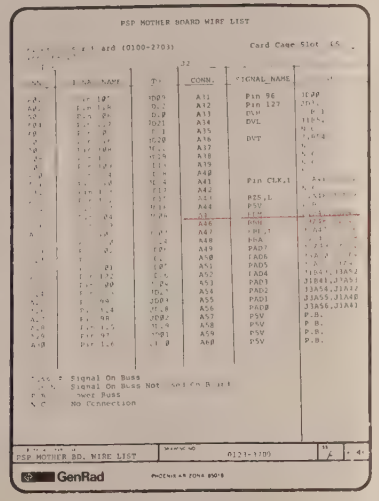
PSP MOTHER BOARD WIRE LIST

PANEL BOARD (0100-2701)

J1 PIN	SIGNAL NAME	J2A PIN	J2B PIN	SIGNAL NAME	TO
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Signal On Buss
Signal On Buss Not Used On Board
Power Buss
No Connection

PSP MOTHER BD. WIRE LIST | DRAWING NO 0123-3700 | GenRad | PHOENIX ARIZONA 85018



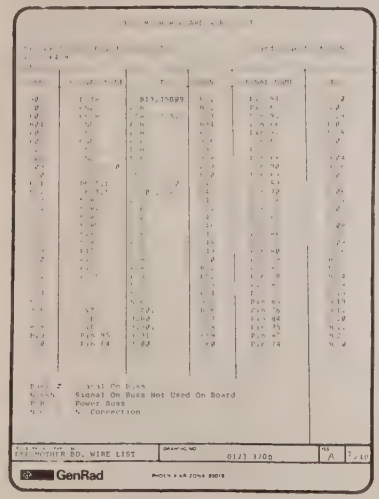
PSP MOTHER BOARD WIRE LIST

Card Cage Slot [illegible]

J1 PIN	SIGNAL NAME	J2 PIN	CONN.	SIGNAL NAME	CONN.
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Signal On Buss
Signal On Buss Not Used On Board
Power Buss
No Connection

PSP MOTHER BD. WIRE LIST | DRAWING NO 0123-3700 | GenRad | PHOENIX ARIZONA 85018



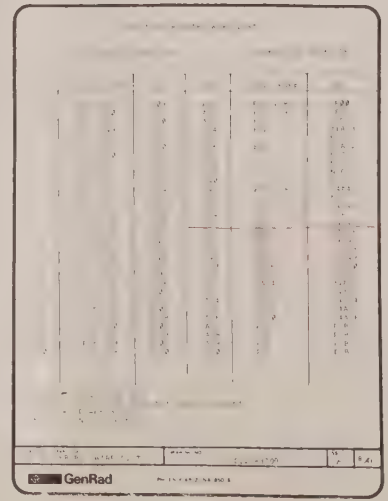
[illegible] MOTHER BOARD WIRE LIST

[illegible] Card (0100-2703)

J1 PIN	SIGNAL NAME	J2 PIN	CONN.	SIGNAL NAME	CONN.
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Signal On Buss
Signal On Buss Not Used On Board
Power Buss
No Connection

PSP MOTHER BD. WIRE LIST | DRAWING NO 0123-3700 | GenRad | PHOENIX ARIZONA 85018



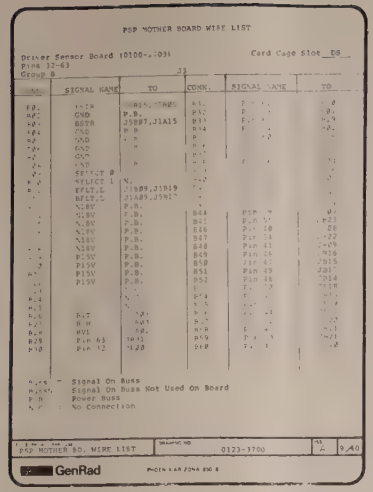
[illegible] MOTHER BOARD WIRE LIST

[illegible] Card (0100-2703)

J1 PIN	SIGNAL NAME	J2 PIN	CONN.	SIGNAL NAME	CONN.
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Signal On Buss
Signal On Buss Not Used On Board
Power Buss
No Connection

[illegible] MOTHER BD. WIRE LIST | DRAWING NO [illegible] | GenRad | PHOENIX ARIZONA 85018



PSP MOTHER BOARD WIRE LIST

Driver Sensor Board (0100-2703)

Card Cage Slot D8

Pins 32-63

Group B

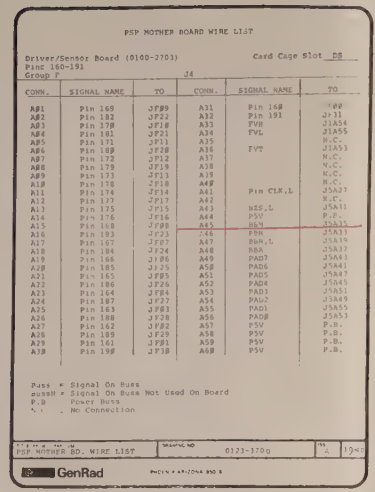
J3

PIN	SIGNAL NAME	TO	CONN.	SIGNAL NAME	TO
B1	FSTR	J1B17,J5B#1	B31		#B
B2	GND	P.B.	B32		P.B.
B3	BSTR	J1B#7,J1A15	B33		
B4	GND	P.B.	B34		
B5	GND		B35		
B6	GND		B36		
B7	GND		B37		
B8	SELECT B		B38		
B9	SELECT A		B39		
B10	EFLT,L	J1B#9,J1B19	B40		
B11	BFLT,L	J1A#9,J5B1	B41		
B12		P.B.	B42		
B13	N18V	P.B.	B43	PIN V	#J
B14	N18V	P.B.	B44	P.B.	P23
B15	N18V	P.B.	B45	P.B.	20
B16	N18V	P.B.	B46	P.B.	22
B17	N18V	P.B.	B47	PIN 41	J#29
B18	P15V	P.B.	B48	PIN 43	J#16
B19	P15V	P.B.	B49	PIN 45	J#15
B20	P15V	P.B.	B50	PIN 47	J#17
B21	P15V	P.B.	B51	PIN 49	J#18
B22	P15V	P.B.	B52	PIN 51	J#14
B23			B53		
B24			B54		
B25			B55		
B26	BVT		B56		
B27	AVM		B57		
B28	AVL		B58		
B29	Pin 63	J#11	B59		
B30	Pin 62	J#20	B60		

#,## = Signal On Buss
#,##N = Signal On Buss Not Used On Board
P.B = Power Buss
N.C = No Connection

PSP MOTHER BD. WIRE LIST | DRAWING NO 0123-3700 | SIZE A | 9/40

GenRad PHOENIX ARIZONA 85018



PSP MOTHER BOARD WIRE LIST

Driver/Sensor Board (0100-2703)

Card Cage Slot D8

Pins 160-191

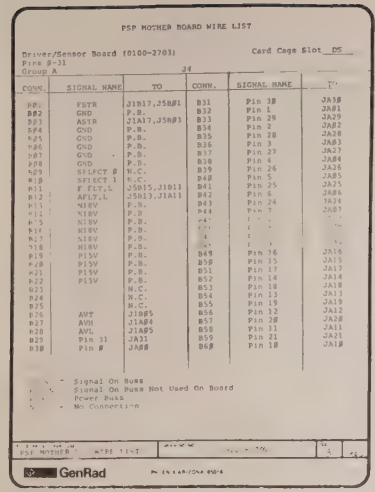
Group F

CONN.	SIGNAL NAME	TO	CONN.	SIGNAL NAME	TO
		J4			
A#1	Pin 169	JF#9	A31	Pin 16#	#9
A#2	Pin 182	JF22	A32	Pin 191	J#11
A#3	Pin 179	JF1#	A33	FVR	J1A54
A#4	Pin 181	JF21	A34	FVL	J1A55
A#5	Pin 171	JF11	A35		N.C.
A#6	Pin 18#	JF2#	A36	FVT	J1A53
A#7	Pin 172	JF12	A37		N.C.
A#8	Pin 179	JF1#	A38		N.C.
A#9	Pin 173	JF13	A39		N.C.
A1#	Pin 178	JF1#	A4#		N.C.
A11	Pin 174	JF14	A41	Pin CLK,L	J5A27
A12	Pin 177	JF17	A42		N.C.
A13	Pin 175	JF15	A43	WZE,L	J5A31
A14	Pin 176	JF16	A44	P5V	P.B.
A15	Pin 168	JF#8	A45	B&W	J5A35
A16	Pin 183	JF23	A46	FBN	J5A33
A17	Pin 167	JF07	A47	B&W,L	J5A39
A18	Pin 184	JF24	A48	B&A	J5A37
A19	Pin 166	JF06	A49	PAD7	J5A43
A2#	Pin 185	JF25	A5#	PAD6	J5A41
A21	Pin 165	JF05	A51	PAD5	J5A47
A22	Pin 186	JF26	A52	PAD4	J5A45
A23	Pin 164	JF04	A53	PAD3	J5A51
A24	Pin 187	JF27	A54	PAD2	J5A49
A25	Pin 163	JF03	A55	PAD1	J5A55
A26	Pin 188	JF28	A56	PAD#	J5A53
A27	Pin 162	JF02	A57	P5V	P.B.
A28	Pin 189	JF29	A58	P5V	P.B.
A29	Pin 161	JF01	A59	P5V	P.B.
A3#	Pin 19#	JF3#	A6#	P5V	P.B.

Buss = Signal On Buss
bussN = Signal On Buss Not Used On Board
P.B = Power Buss
N.C. = No Connection

PSP MOTHER BD. WIRE LIST | DRAWING NO 0123-3700 | SIZE A | 10/40

GenRad PHOENIX ARIZONA 85018



PSP MOTHER BOARD WIRE LIST

Driver/Sensor Board (0100-2703)

Card Cage Slot D5

Pins 0-31

Group A

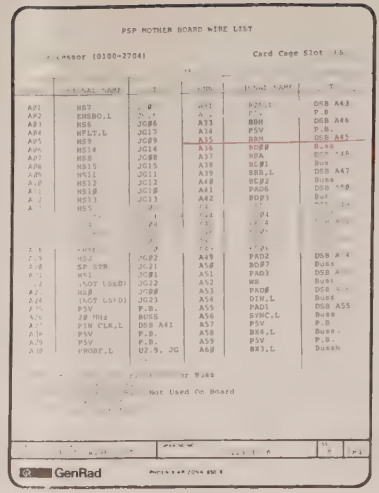
J4

CONN.	SIGNAL NAME	TO	CONN.	SIGNAL NAME	TO
B#1	FSTR	J1B17,J5B#1	B31	Pin 1#	JA1#
B#2	GND	P.B.	B32	Pin 1	JA#1
B#3	ASTR	J1A17,J5B#3	B33	Pin 29	JA29
B#4	GND	P.B.	B34	Pin 2	JA#2
B#5	GND	P.B.	B35	Pin 28	JA28
B#6	GND	P.B.	B36	Pin 3	JA#3
B#7	GND	P.B.	B37	Pin 27	JA27
B#8	GND	P.B.	B38	Pin 4	JA#4
B#9	SELECT B	N.C.	B39	Pin 26	JA26
B1#	SELECT A	N.C.	B4#	Pin 5	JA#5
B11	E FLT,L	J5B15,J1B11	B41	Pin 25	JA25
B12	AFLT,L	J5B13,J1A11	B42	Pin 6	JA#6
B13	N18V	P.B.	B43	Pin 24	JA24
B14	N18V	P.B.	B44	Pin 7	JA#7
B15	N18V	P.B.	B45		
B16	N18V	P.B.	B46		
B17	N18V	P.B.	B47		
B18	N18V	P.B.	B48		
B19	P15V	P.B.	B49	Pin 36	JA36
B2#	P15V	P.B.	B5#	Pin 15	JA15
B21	P15V	P.B.	B51	Pin 17	JA17
B22	P15V	P.B.	B52	Pin 14	JA14
B23		N.C.	B53	Pin 18	JA18
B24		N.C.	B54	Pin 13	JA13
B25		N.C.	B55	Pin 19	JA19
B26	AVT	J1B#5	B56	Pin 12	JA12
B27	AVM	J1A#4	B57	Pin 2#	JA2#
B28	AVL	J1A#5	B58	Pin 11	JA11
B29	Pin 31	JA31	B59	Pin 21	JA21
B3#	Pin #	JA##	B6#	Pin 1#	JA1#

#,## = Signal On Buss
#,##N = Signal On Buss Not Used On Board
P.B = Power Buss
N.C = No Connection

PSP MOTHER [illegible] | SIZE A | 5/40

GenRad PHOENIX ARIZONA 85018

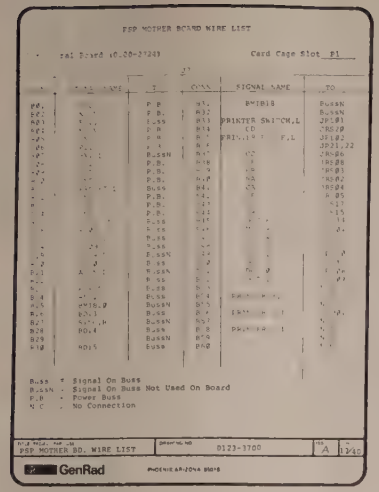


PSP MOTHER BOARD WIRE LIST

[illegible] Sensor (0100-2704)

Card Cage Slot [illegible]

CONN.	SIGNAL NAME	TO	CONN.	SIGNAL NAME	TO
A#1	HS7	[illegible]	[illegible]	[illegible]	DSB A43
A#2	EMSB0,L	[illegible]	[illegible]	[illegible]	P.B.
A#3	HS6	JG#6	A33	BBH	DSB A46
A#4	HFLT,L	JG17	A34	P5V	P.B.
A#5	HS9	JG#9	A35	BBM	DSB A45
A#6	HS14	JG14	A36	BOF#	Buss
A#7	HS8	JG#8	A37	BDA	DSB [illegible]
A#8	HS15	JG15	A38	BC,#1	Buss
A#9	HS11	JG11	A39	BBB,L	DSB A47
A1#	HS12	JG12	A4#	BC,#2	Buss
A11	HS1#	JG1#	A41	PAD6	DSB [illegible]
A12	HS13	JG13	A42	BOF3	Buf
A13	HS5	JG05	A43	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]



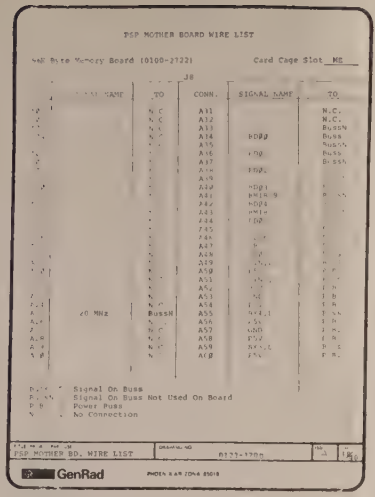
PSP MOTHER BOARD WIRE LIST

Card Cage Slot P1

Buss = Signal On Buss
BussN = Signal On Buss Not Used On Board
P.B. = Power Buss
N.C. = No Connection

PSP MOTHER BD. WIRE LIST | 0123-3700 | A

GenRad



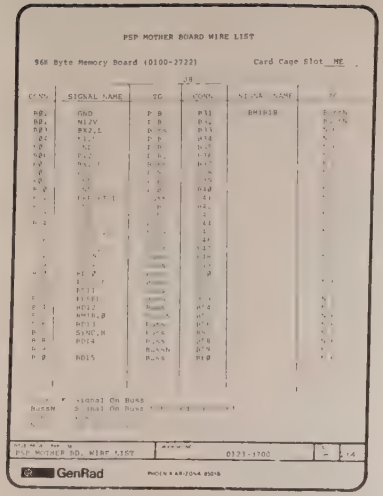
PSP MOTHER BOARD WIRE LIST

Card Cage Slot ME

Buss = Signal On Buss
BussN = Signal On Buss Not Used On Board
P.B. = Power Buss
N.C. = No Connection

PSP MOTHER BD. WIRE LIST | 0123-3700

GenRad

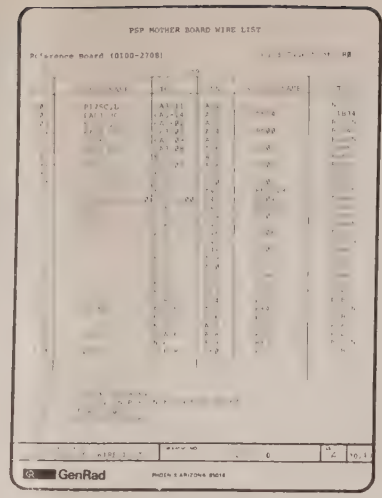


PSP MOTHER BOARD WIRE LIST

$6K Byte Memory Board (0100-2722)

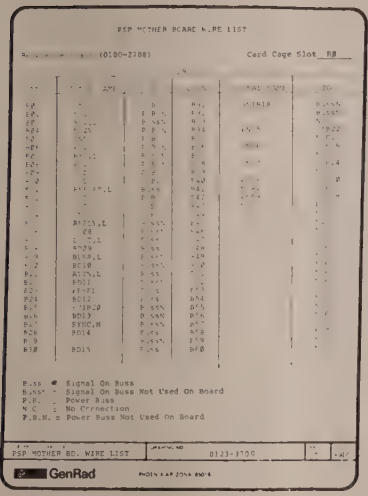
Card Cage Slot ME

GenRad



PSP MOTHER BOARD WIRE LIST

GenRad



PSP MOTHER BOARD WIRE LIST

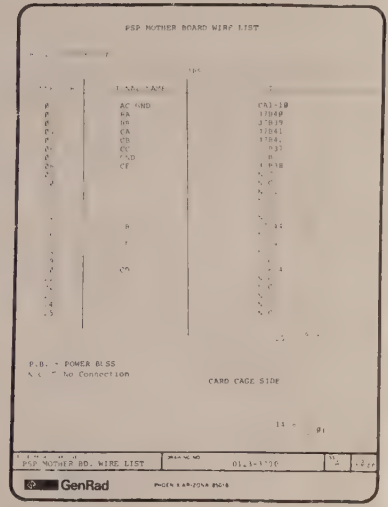
(0100-2708)

Card Cage Slot P8

Buss = Signal On Buss
BussN = Signal On Buss Not Used On Board
P.B. = Power Buss
N.C. = No Connection
P.B.N. = Power Buss Not Used On Board

PSP MOTHER BD. WIRE LIST | 0123-3700

GenRad



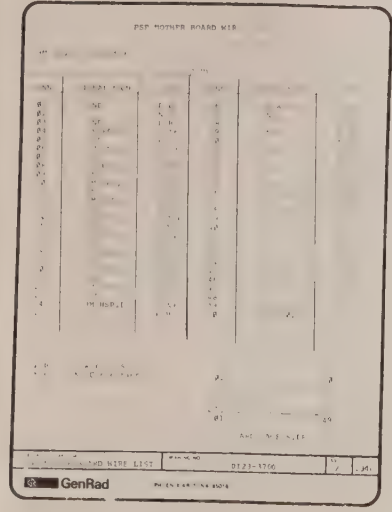
PSP MOTHER BOARD WIRE LIST

P.B. - POWER BUSS
N.C. - No Connection

CARD CAGE SIDE

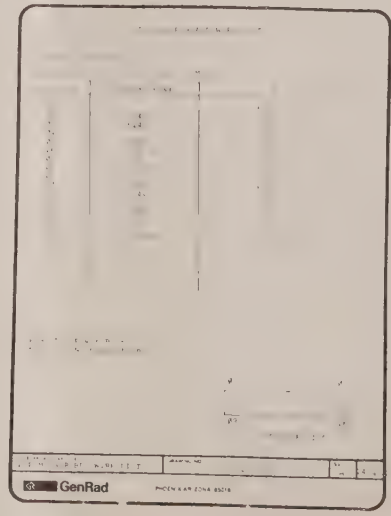
PSP MOTHER BD. WIRE LIST

GenRad

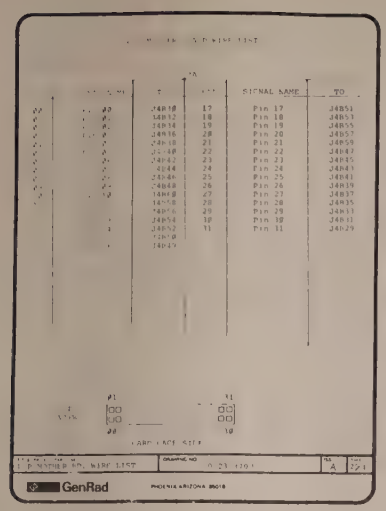


PSP MOTHER BOARD WIR

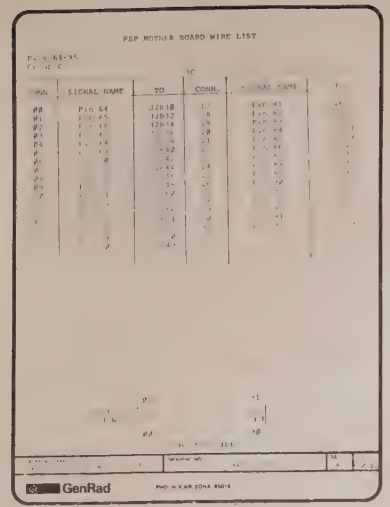
GenRad

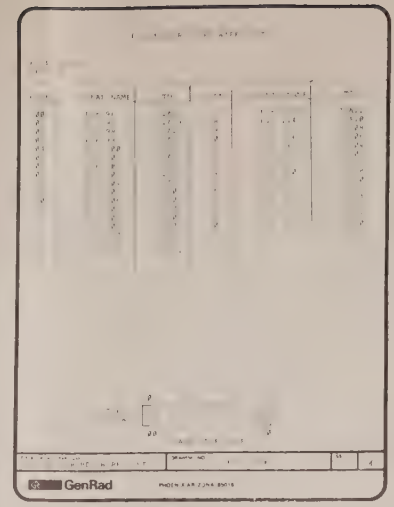


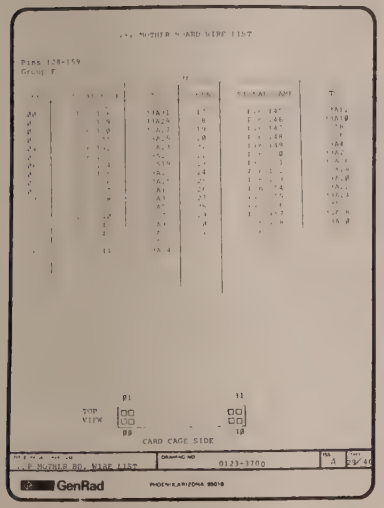
GenRad

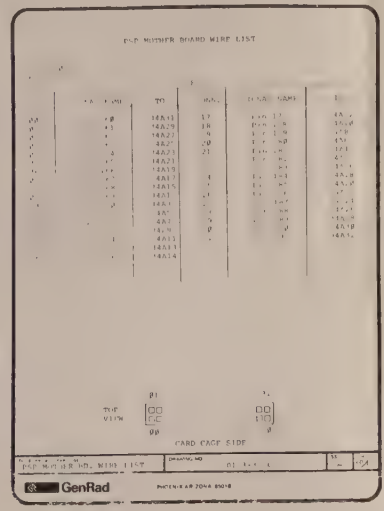

SIGNAL NAME
TO
Pin 17
Pin 18
Pin 19
Pin 20
Pin 21
Pin 22
Pin 23
Pin 24
Pin 25
Pin 26
Pin 27
Pin 28
Pin 29
Pin 30
Pin 31
CARD CAGE SIDE
GenRad

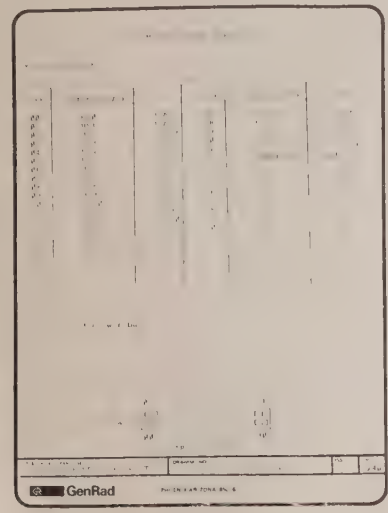
PSP MOTHER BOARD WIRE LIST
CARD CAGE SIDE
GenRad

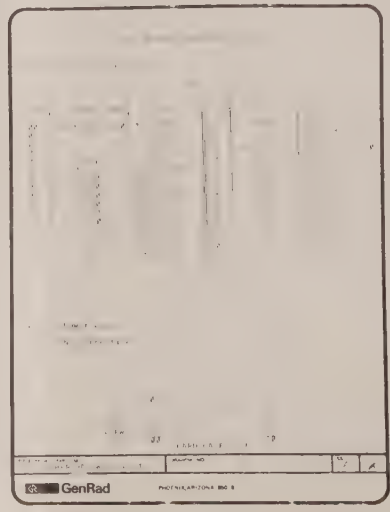

PSP MOTHER BOARD WIRE LIST
SIGNAL NAME
TO
CONN.
GenRad


GenRad


Pins 128-159
Group F
CARD CAGE SIDE
GenRad


PSP MOTHER BOARD WIRE LIST
CARD CAGE SIDE
GenRad


GenRad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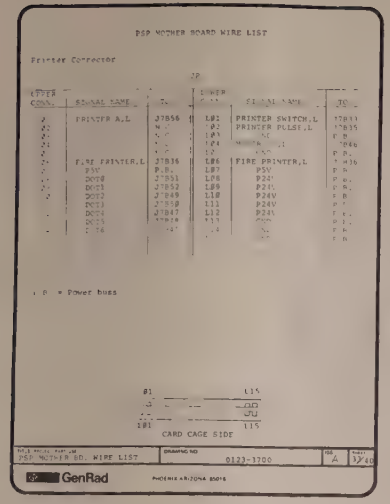

PSP MOTHER BOARD WIRE LIST

Printer Connector

J2

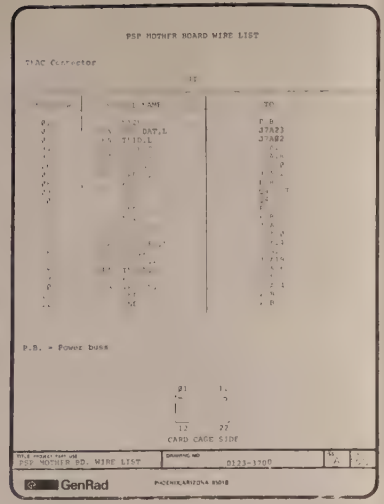
UPPER CONN.	SIGNAL NAME	TO	LOWER CONN.	SIGNAL NAME	TO
A	PRINTER A,L	J7B56	L01	PRINTER SWITCH,L	J7B33
B02			L02	PRINTER PULSE,L	J7B35
C03			L03	NC	P.B.
D04			L04		J7B46
E			L05		P.B.
F06	FIRE PRINTER,L	J7B36	L06	FIRE PRINTER,L	J7A36
H07	P5V	P.B.	L07	P5V	P.B.
J08	DOT8	J7B51	L08	P24V	P.B.
K09	DOT7	J7B52	L09	P24V	P.B.
L10	DOT2	J7B49	L10	P24V	P.B.
M11	DOT3	J7B50	L11	P24V	P.B.
N12	DOT4	J7B47	L12	P24V	P.B.
P13	DOT5	J7B48	L13	P5V	P.B.
R14	DOT6	J7B45	L14	P5V	P.B.

P.B. = Power buss

CARD CAGE SIDE

PSP MOTHER BD. WIRE LIST | 0123-3700 | A | 1/2

GenRad PHOENIX,ARIZONA 85018


PSP MOTHER BOARD WIRE LIST

THAC Connector

J2

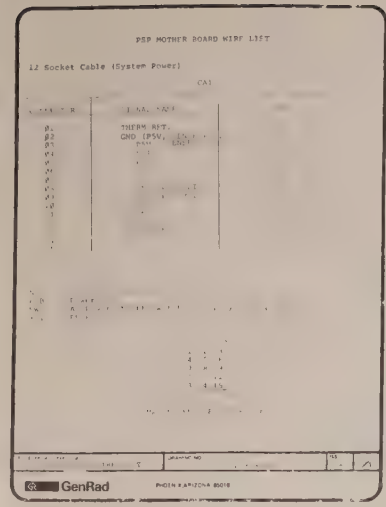
	NAME	TO
P.B.		P.B.
J	DAT,L	J7A23
K	TIID,L	J7A02

P.B. = Power buss

CARD CAGE SIDE

PSP MOTHER BD. WIRE LIST | 0123-3700 | A | 1/2

GenRad PHOENIX,ARIZONA 85018

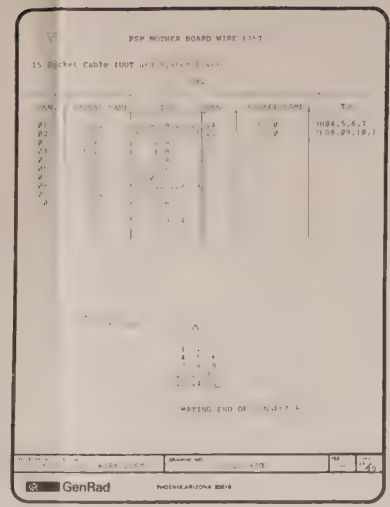

PSP MOTHER BOARD WIRE LIST

12 Socket Cable (System Power)

CA1

	NAME	TO
P.B.		P.B.
P2	THERM ART.	
P3	GND (P5V,	

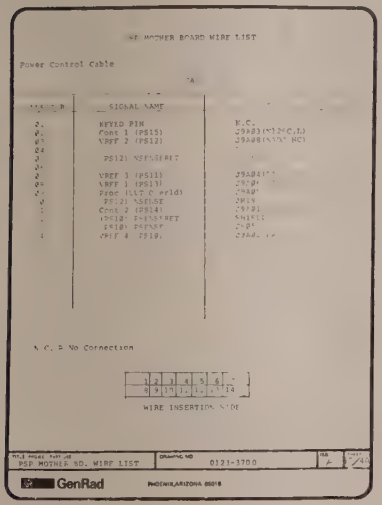
GenRad PHOENIX,ARIZONA 85018


PSP MOTHER BOARD WIRE LIST

15 Socket Cable (OUT

MATING END OF

GenRad PHOENIX,ARIZONA 85018


PSP MOTHER BOARD WIRE LIST

Power Control Cable

CA

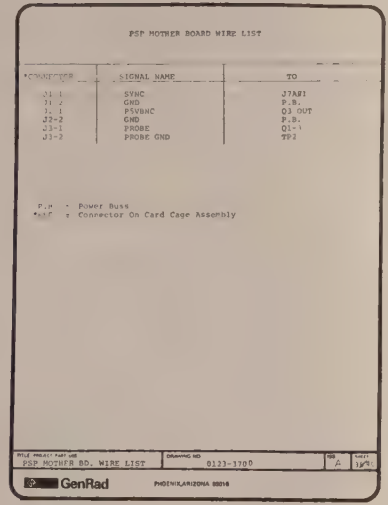
P	SIGNAL NAME	
J.	KEYED PIN	N.C.
K.	Cont 1 (PS15)	J9A83(+12V,C,E)
L.	VRT 2 (PS12)	J9A84(+5V, HC)
M.		
N.	PS12) VERT/SERET	
P.		
R.	VRT 3 (PS11)	J9A85(+
S.	VRT 1 (PS13)	J9A9(
T.	Proc (LLT C erid)	J9A8(
U.	PS12) SELESE	J9A9
V.	Cont 2 (PS14)	J9A91
W.	(PS13) SELESERET	J9A10
X.	(PS10) P5VSEF	J9A(
Y.	VRT 4 PS10)	J9A8(

N.C. = No Connection

WIRE INSERTION SIDE

PSP MOTHER BD. WIRE LIST | 0123-3700 | A | 1/2

GenRad PHOENIX,ARIZONA 85018


PSP MOTHER BOARD WIRE LIST

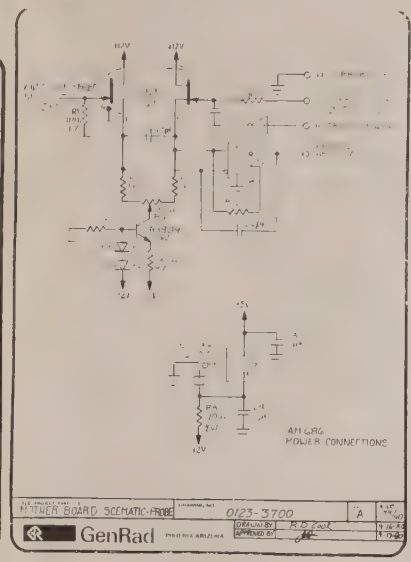
CONNECTOR	SIGNAL NAME	TO
J1-1	SYNC	J7A81
J1-2	GND	P.B.
J1-1	PSVBNC	Q3 OUT
J2-2	GND	P.B.
J3-1	PROBE	Q1-1
J3-2	PROBE GND	TP2

P.B. = Power Buss

* = Connector On Card Cage Assembly

PSP MOTHER BD. WIRE LIST | 0123-3700 | A | 1/2

GenRad PHOENIX,ARIZONA 85018


+12V

R1

AMGRG

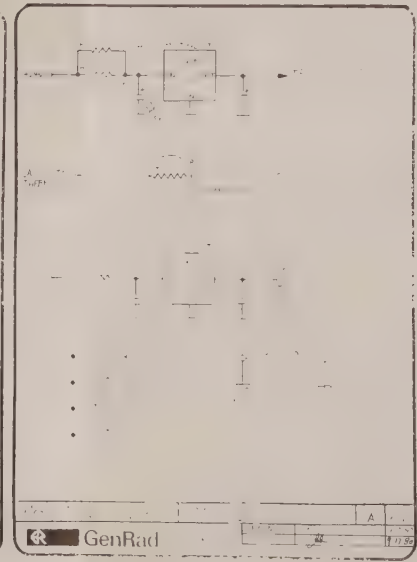
POWER CONNECTIONS

MOTHER BOARD SCEMATIC-PROBE | 0123-3700 | A

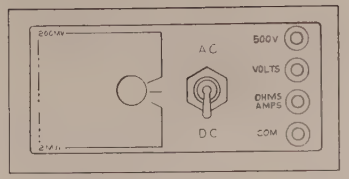
GenRad PHOENIX,ARIZONA

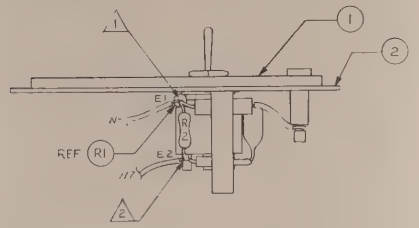
DRAWN BY R.S.Zack

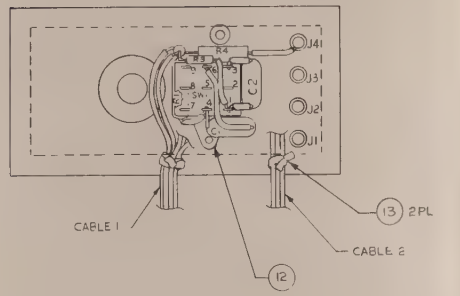
APPROVED BY


GenRad

REVISION				
ISSUE	RELEASE NO	DATE	APPD	DESCRIPTION
L		SEP 83	RAM	REVIEWED & REDRAWN PER ENG NOTEBOOK NO. P005







WIRE LIST

WIRE No.	ITEM No.	AWG COLOR	CUT LENGTH	FROM	TERM	TO	TERM
W1	ITEM 9	24 BU	3.50	SW1-8	SOL	CABLE 2	3
W2	ITEM 10	24 VT	3.75	SW1-7	SOL	CABLE 2	3
W3	ITEM 8	24 GN	3.25	SW1-9	SOL	CABLE 2	3
W4	ITEM 1	24 WH	1.50	SW1-5	SOL	J1	SOL
W5	ITEM 11	24 WH	1.50	SW1-2	SOL	J2	SOL
W6	ITEM 11	24 WH	3.25	SW1-1	SOL	CABLE 1	3
W7	ITEM 7	24 YL	3.25	E2 2	SOL	CABLE 1	3
W8	ITEM 6	24 OR	3.50	E1 1	SOL	CABLE 1	3
W9	ITEM 5	24 RD	2.25	J4	SOL	CABLE 2	3
W10	ITEM 4	24 BN	3.75	J3	SOL	CABLE 1	3
W11	ITEM 3	24 BK	2.00	IT12	SOL	CABLE 1	3

COMPONENT CONNECTION

COMP	LEAD DESIG	TO	SLEEVING	TERM
C1	A	SW1-4	N/A	SOL
	B	SW1-6	ITEM 10	
C2	A	SW1-1	ITEM 6	
	B	SW1-3	ITEM 10	
R1	A	SW1-4	ITEM 10	
	B	E1 1	N/A	
R2	A	E2 2	N/A	
	B	E1 1	N/A	
R3	A	E2 2	N/A	
	B	SW1-1	ITEM 6	
R4	A	J4	ITEM 6	
	B	E1 1	N/A	SOL

3 STRIP & TIN LOOSE ENDS OF ALL WIRES .25±.12.

2 E2 IS DEFINED AS THE POINT AT WHICH R2A, R3A & W7 MEET & ARE SOLDERED

1 E1 IS DEFINED AS THE POINT AT WHICH COMP LEADS R4B, R2B, R1B & W8 MEET & ARE SOLDERED

NOTES

UNLESS OTHERWISE SPECIFIED

DRAWN RAM 9-15-83

TOLERANCE

SIZE A

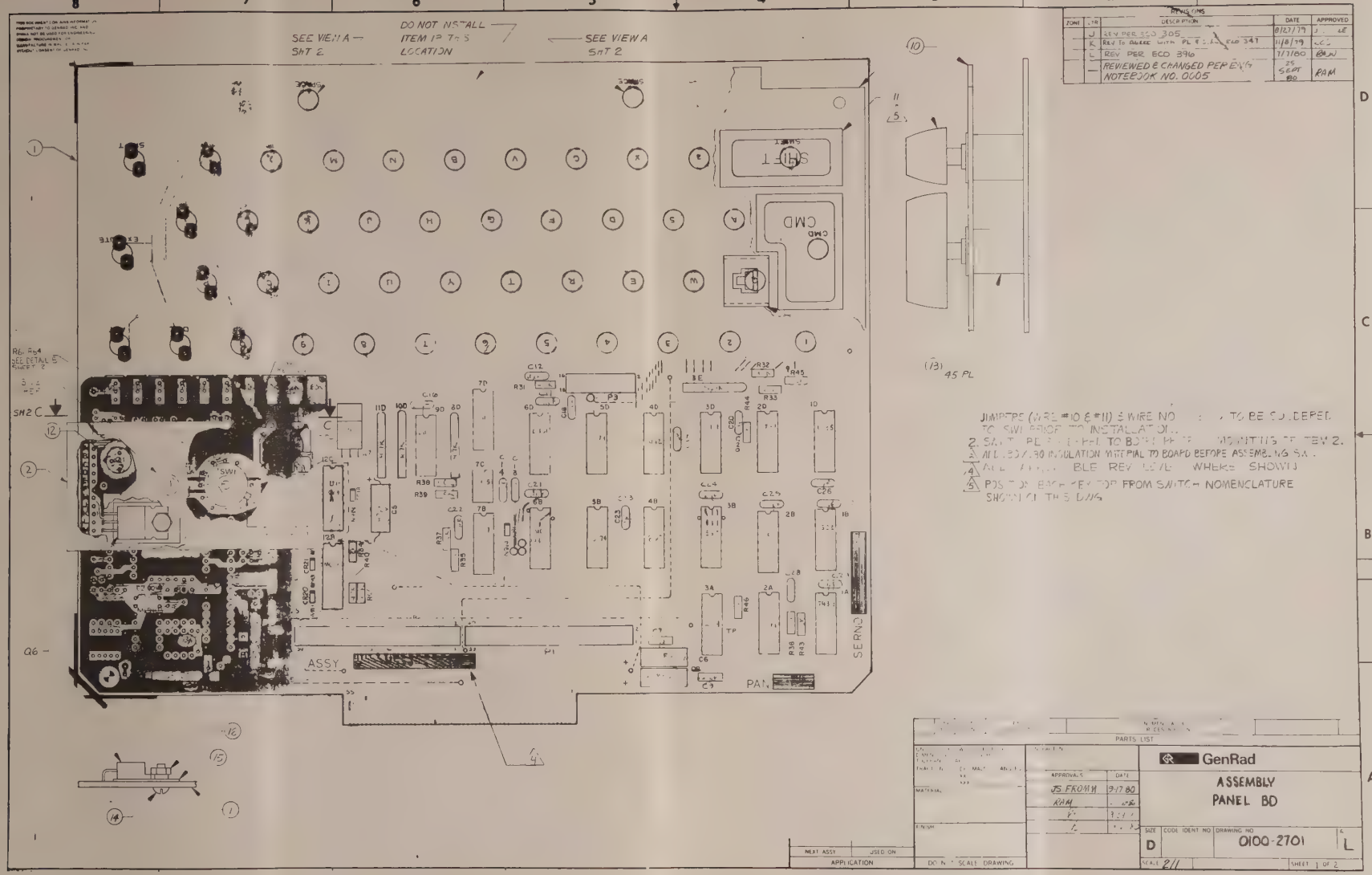
SCALE 2

TITLE ASSY, DMM

GenRad PHOENIX ARIZONA 85016

DRAWING NO. 0100-2002/L

1/1

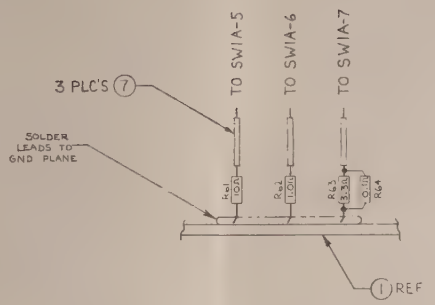

SEE VIEW A SHT 2
DO NOT INSTALL ITEM IN THIS LOCATION
SEE VIEW A SHT 2
SHIFT
CMD
45 PL
JUMPERS (WIRE #10 & #11) & WIRE NO TO BE SOLDERED TO SWITCH PRIOR TO INSTALLATION.
SAME AS ITEM 1 EXCEPT TO BOARD PRIOR TO MOUNTING OF ITEM 2.
ALL 330 INSULATION MATERIAL TO BOARD BEFORE ASSEMBLING SX.
ALL PARTS TO BE REV LEVEL WHERE SHOWN
POSITION BACK REV TOP FROM SWITCH NOMENCLATURE SHOWN ON THIS DWG
ASSY
PAT
SERNO
PARTS LIST
GenRad
ASSEMBLY
PANEL BD
0100-2701
SIZE D
SCALE 2/1
SHEET 1 OF 2
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	J	REV PER ECO 305	8/27/79	LE
	K	REV TO AGREE WITH PL & LAYOUT ECO 347	11/8/79	LCL
	L	REV PER ECO 396	7/7/80	BWN
	—	REVIEWED & CHANGED PER ENG NOTEBOOK NO. 0005	25 SEPT 80	RAM

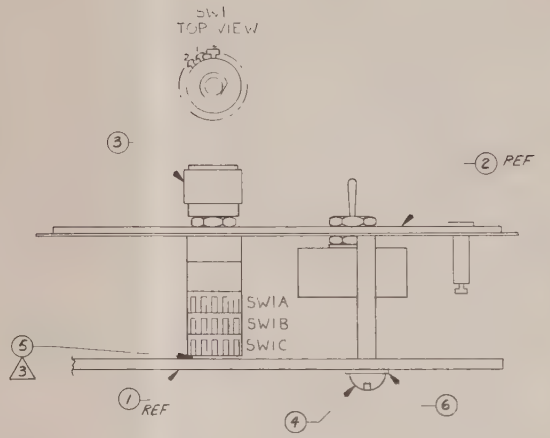
REVISION				
ISSUE	REL'CN NO	DATE	APPD	DESCRIPTION
L	SEE SHEET 1			

WIRE CONNECTION LIST

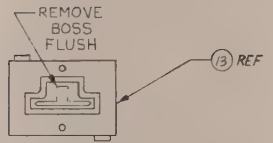
WIRE #	ITEM OR COLOR	FROM	TO	
1	BLK	GND LUG UNDER SW2	SWIC-12	
2	BRN	ITEM 2	SWIA-1	
3	RED	ITEM 2	TERMINATION F	
4	ORG	ITEM 2	SWIA-4	
5	YLW	ITEM 2	SWIA-3	
6	WHT	ITEM 2	SWIA-2	
7	GRN	ITEM 2	TERMINATION L	
8	VIO	SW2A-DC	TERMINATION K	
9	BLU	SW2A-COM	TERMINATION M	
10	ITEM 9 (JUMPER)	SWIA-1	SWIA-2	2
11	ITEM 9 (JUMPER)	SWIB-5	SWIB-6,7&8	2
12	ITEM 8 (28 AWG)	SWIA-8	TERMINATION D	4
13		SWIA-9	A	
14		SWIA-10	C	
15		SWIA-11	B	
16		SWIA-12	E	
17		SWIB-12	H	
18		SWIB-8	TERMINATION J	
19	ITEM 8	SWIB-1	SWIB-5	



DETAIL B

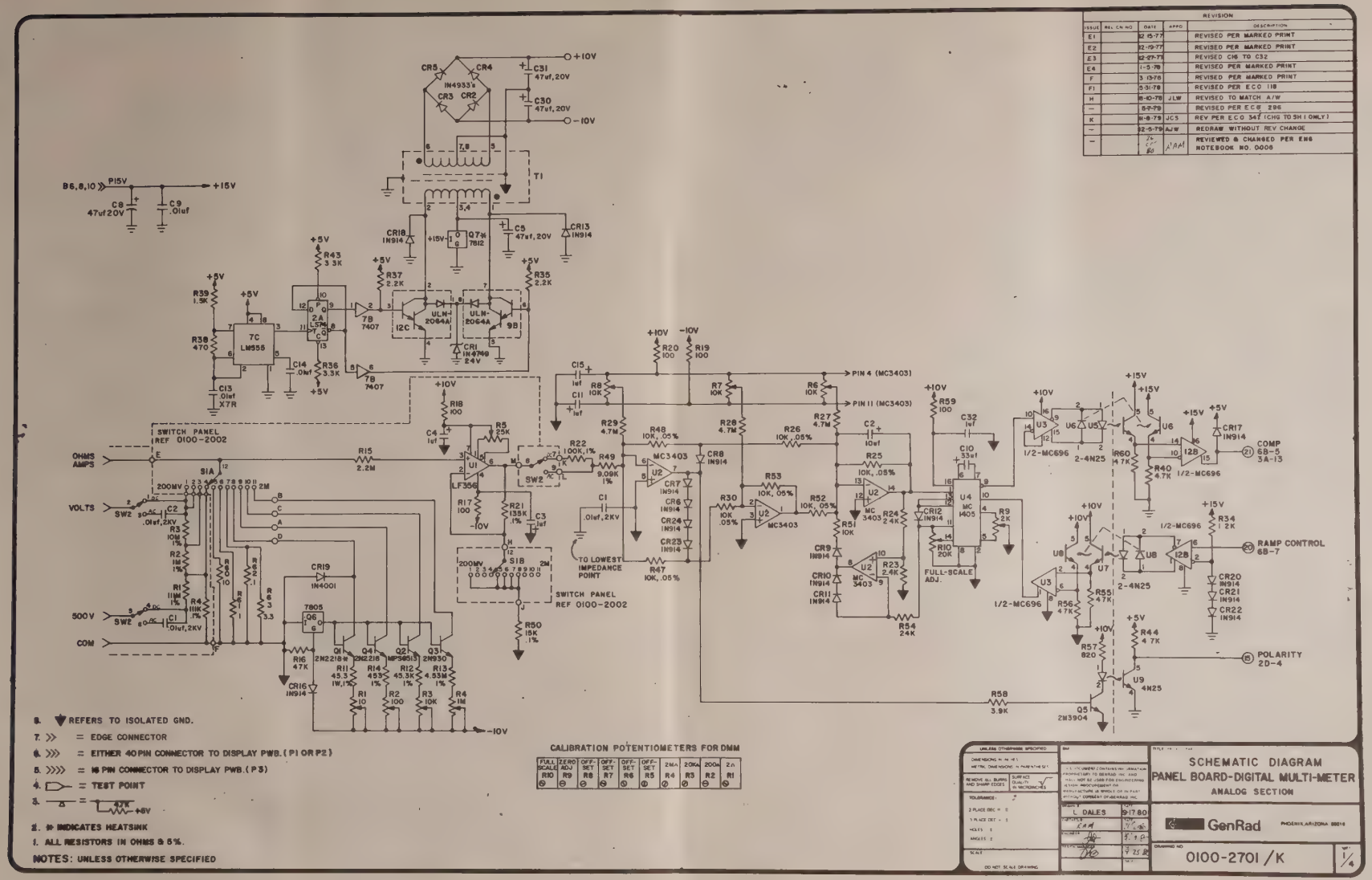


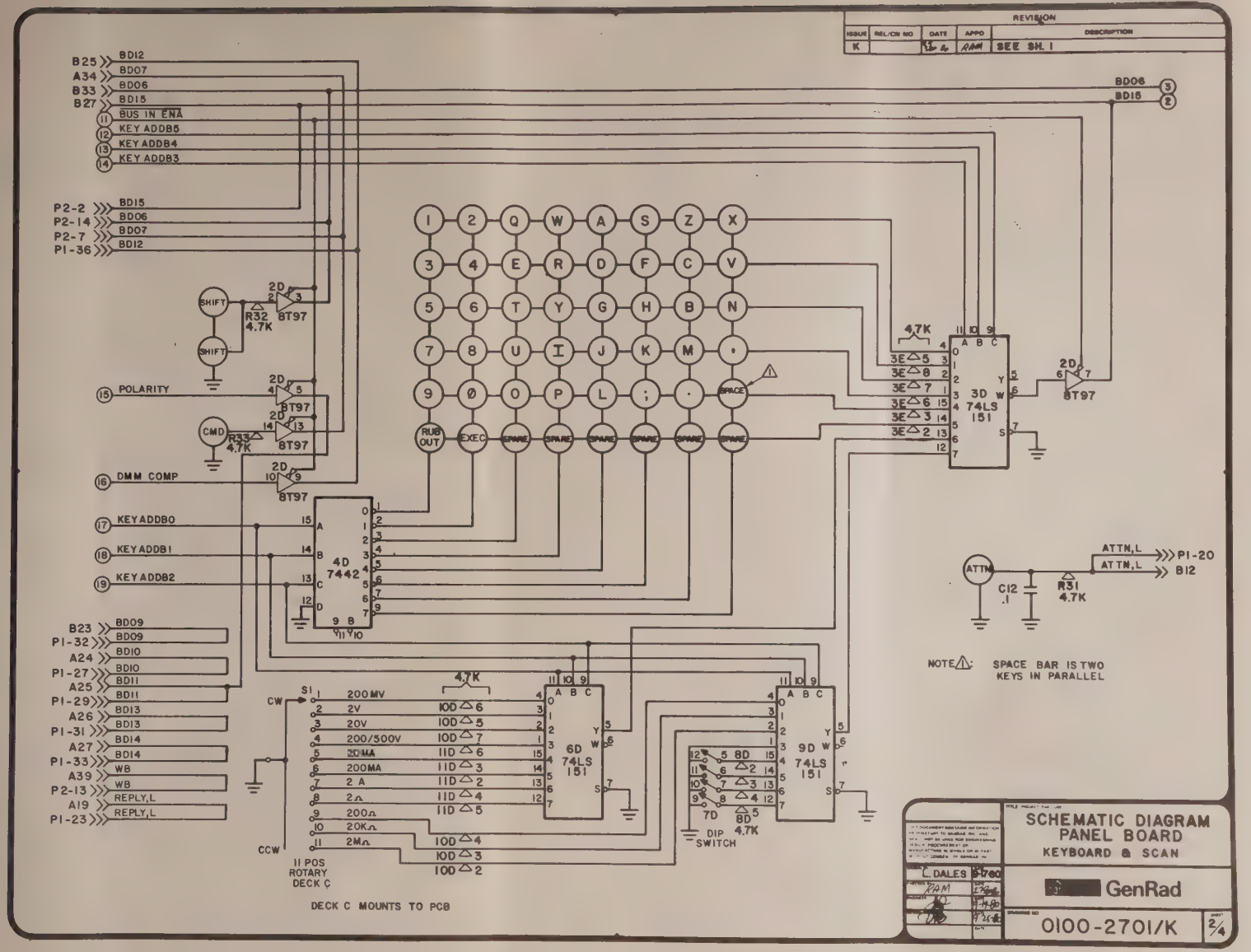
VIEW C-C
ROTATED 180°

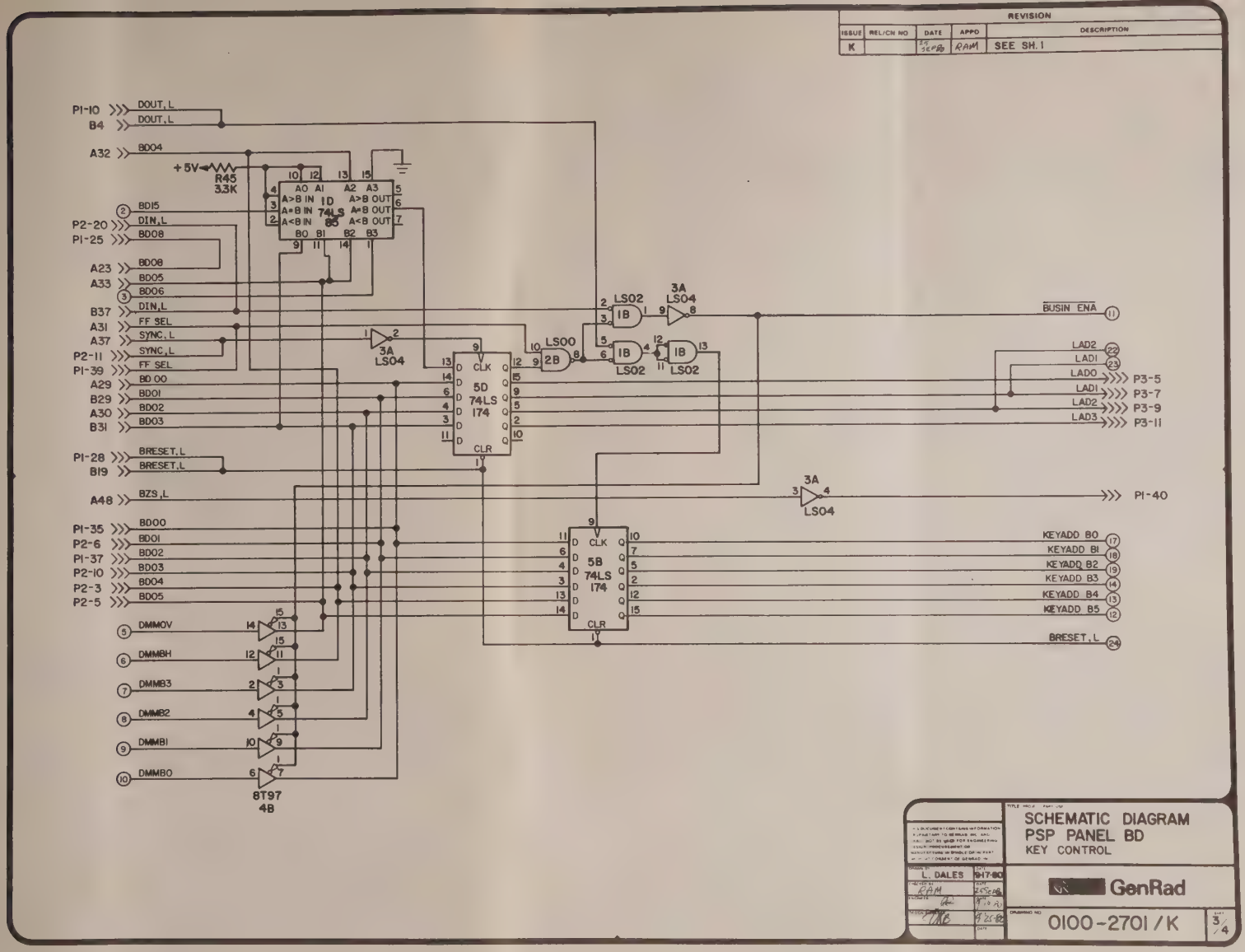


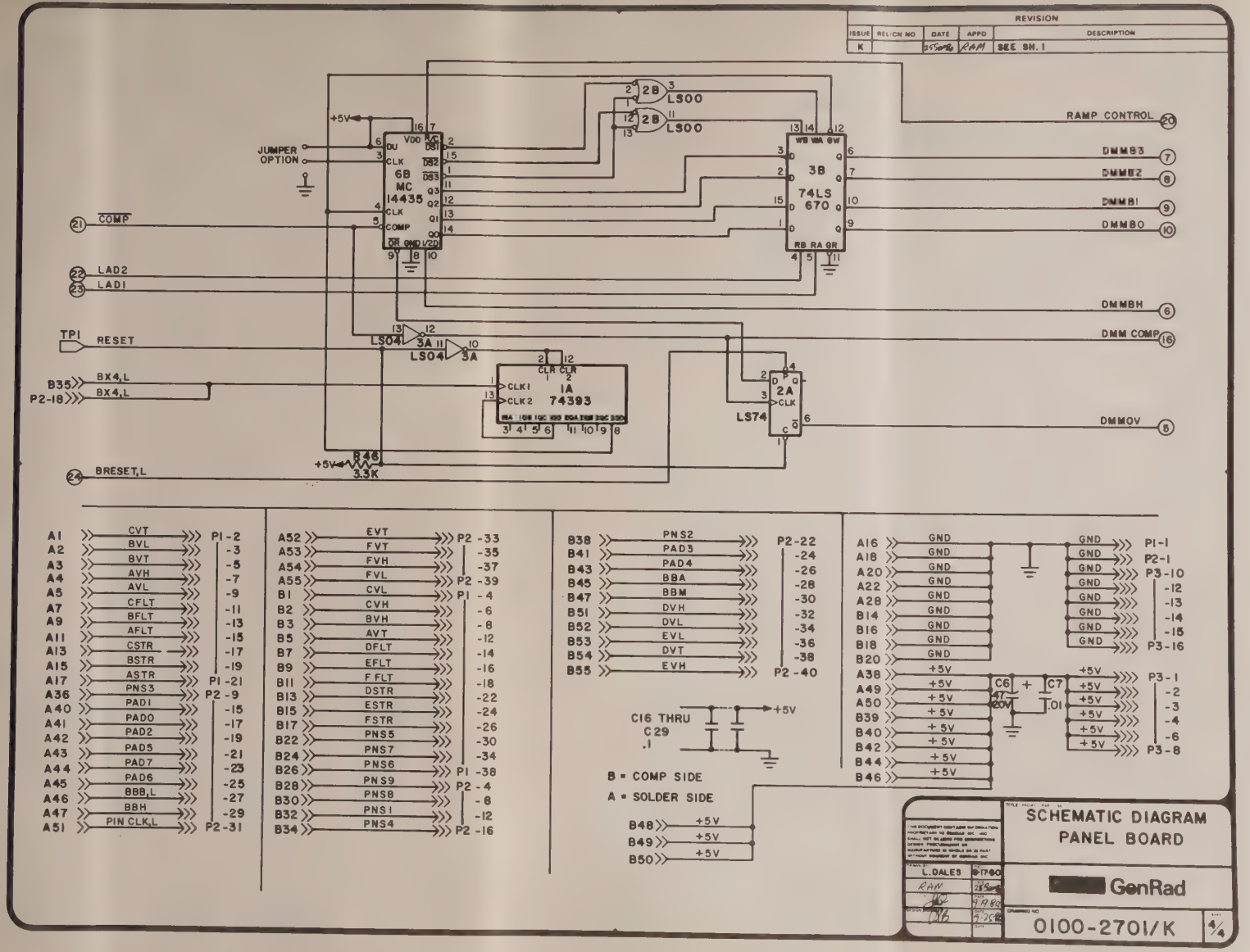
VIEW A
(SWITCH)
2 PL

UNLESS OTHERWISE SPECIFIED	BM	TITLE
REMOVE ALL BURR AND SHARP EDGE		ASSEMBLY PANEL BOARD
TOLERANCE	JS FROMM 7-2-80	GenRad PHOENIX ARIZONA 85018
NEXT ASSY NONE	RAM 7-2-80	DRAWING NO. 0100-2701/L 3/3

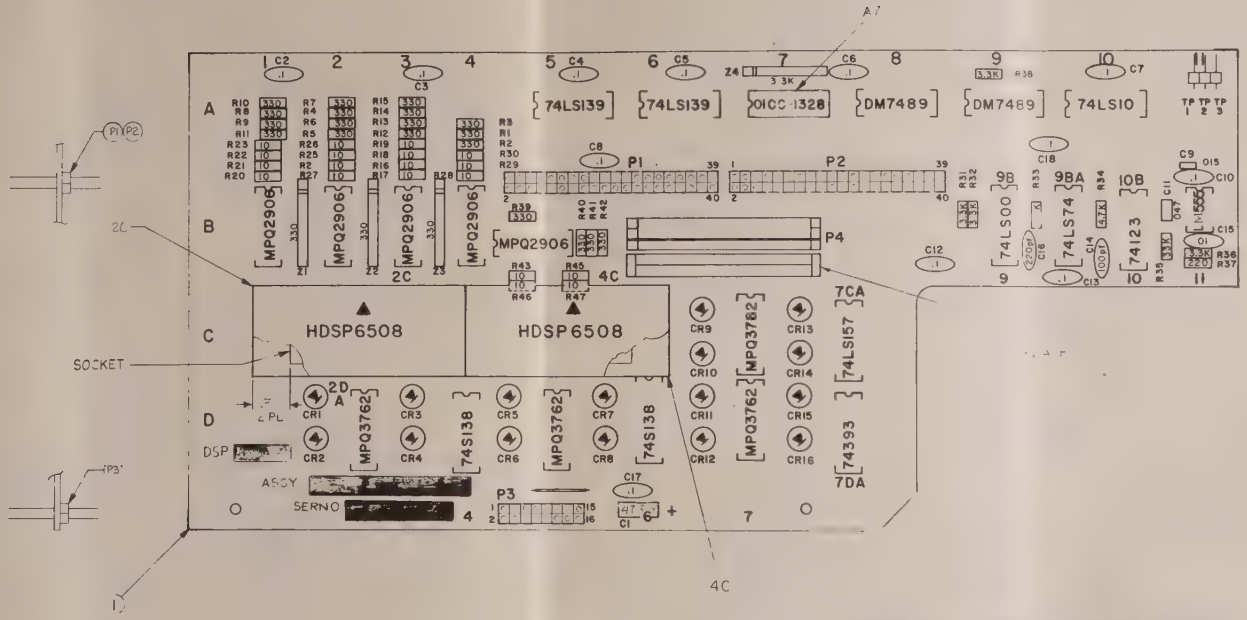

REVISION
ISSUE REL. CN NO. DATE APPD DESCRIPTION
E1 12-15-77 REVISED PER MARKED PRINT
E2 12-19-77 REVISED PER MARKED PRINT
E3 12-27-77 REVISED CH5 TO C32
E4 1-5-78 REVISED PER MARKED PRINT
F 3-13-78 REVISED PER MARKED PRINT
F1 3-31-78 REVISED PER ECO 118
H 8-10-78 JLW REVISED TO MATCH A/W
— 5-3-79 REVISED PER ECO 286
K 11-8-79 JCS REV PER ECO 347 (CHG TO SH 1 ONLY)
— 12-5-79 AJW REDRAW WITHOUT REV CHANGE
— 2-6-80 AAM REVIEWED & CHANGED PER ENG NOTEBOOK NO. 0008
SCHEMATIC DIAGRAM
PANEL BOARD-DIGITAL MULTI-METER
ANALOG SECTION
GenRad
PHOENIX, ARIZONA 85018
0100-2701 /K
1/4
L. DALES 9-17-80
CALIBRATION POTENTIOMETERS FOR DMM
FULL SCALE R10 ZERO ADJ R9 OFF-SET R8 OFF-SET R7 OFF-SET R6 OFF-SET R5 2MA R4 20KA R3 200A R2 2A R1
SWITCH PANEL REF 0100-2002
OHMS AMPS
VOLTS
500V
COM
TO LOWEST IMPEDANCE POINT
FULL-SCALE ADJ.
COMP 6B-5 3A-13
RAMP CONTROL 6B-7
POLARITY 2D-4
8. REFERS TO ISOLATED GND.
7. = EDGE CONNECTOR
6. = EITHER 40 PIN CONNECTOR TO DISPLAY PWB. (P1 OR P2)
5. = 16 PIN CONNECTOR TO DISPLAY PWB. (P3)
4. = TEST POINT
3. = 47K +6V
2. ⊕ INDICATES HEATSINK
1. ALL RESISTORS IN OHMS & 5%.
NOTES: UNLESS OTHERWISE SPECIFIED


REVISION
ISSUE K
REL/CN NO
DATE
APPD
DESCRIPTION
SEE SH. 1
B25 BD12
A34 BD07
B33 BD06
B27 BD15
11 BUS IN ENA
12 KEY ADDB5
13 KEY ADDB4
14 KEY ADDB3
P2-2 BD15
P2-14 BD06
P2-7 BD07
P1-36 BD12
BD06
BD15
SHIFT
SHIFT
R32 4.7K
8T97
15 POLARITY
CMD
R33 4.7K
16 DMM COMP
17 KEY ADDB0
18 KEY ADDB1
19 KEY ADDB2
4D 7442
B23 BD09
P1-32 BD09
A24 BD10
P1-27 BD10
A25 BD11
P1-29 BD11
A26 BD13
P1-31 BD13
A27 BD14
P1-33 BD14
A39 WB
P2-13 WB
A19 REPLY,L
P1-23 REPLY,L
I 2 Q W A S Z X
3 4 E R D F C V
5 6 T Y G H B N
7 8 U I J K M ,
9 Ø O P L ; . SPACE
RUB OUT
EXEC
SPARE
4.7K
3D 74LS 151
ATTN,L
ATTN,L
P1-20
B12
ATTN
C12 .1
R31 4.7K
NOTE SPACE BAR IS TWO KEYS IN PARALLEL
S1
CW
CCW
200MV
2V
20V
200/300V
50MA
200MA
2 A
2Ω
200Ω
20KΩ
2MΩ
11 POS ROTARY DECK C
DECK C MOUNTS TO PCB
6D 74LS 151
9D 74LS 151
8D
7D
DIP SWITCH
SCHEMATIC DIAGRAM
PANEL BOARD
KEYBOARD & SCAN
L. DALES
GenRad
0100-2701/K
2/4


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
K | | 25 SEP 80 | RAM | SEE SH. 1
P1-10 DOUT,L
B4 DOUT,L
A32 BD04
+5V R45 3.3K
10D 74LS 85
A0 A1 A2 A3
A>B IN A=B IN A<B IN
A>B OUT A=B OUT A<B OUT
B0 B1 B2 B3
BD15
P2-20 DIN,L
P1-25 BD08
A23 BD08
A33 BD05
BD06
B37 DIN,L
A31 FF SEL
A37 SYNC,L
P2-11 SYNC,L
P1-39 FF SEL
A29 BD 00
B29 BD01
A30 BD02
B31 BD03
P1-28 BRESET,L
B19 BRESET,L
A48 BZS,L
P1-35 BD00
P2-6 BD01
P1-37 BD02
P2-10 BD03
P2-3 BD04
P2-5 BD05
DMMOV
DMMBH
DMMB3
DMMB2
DMMB1
DMMB0
8T97 4B
3A LS04
LS02 1B
LS00 2B
5D 74LS 174
5B 74LS 174
CLK CLR
BUSIN ENA
LAD2
LAD1
LAD0
LAD1
LAD2
LAD3
P3-5
P3-7
P3-9
P3-11
P1-40
KEYADD B0
KEYADD B1
KEYADD B2
KEYADD B3
KEYADD B4
KEYADD B5
BRESET,L
SCHEMATIC DIAGRAM
PSP PANEL BD
KEY CONTROL
L. DALES
RAM
GenRad
0100-2701/K
3/4


REVISION
ISSUE | REL-CN NO | DATE | APPD | DESCRIPTION
K | | 3-5-86 | RAM | SEE SH. 1
+5V
JUMPER OPTION
6B MC 14435
74LS 670
38
LS00
LS04
LS74
74393
1A
2A
3A
RAMP CONTROL
DMMB3
DMMB2
DMMB1
DMMB0
DMMBH
DMM COMP
DMMOV
COMP
LAD2
LADI
TPI
RESET
BX4,L
B35
P2-18
BRESET,L
R46
3.3K
C16 THRU C29 .1
C6 47 20V
C7 .01
B = COMP SIDE
A = SOLDER SIDE
A1 CVT P1-2
A2 BVL -3
A3 BVT -5
A4 AVH -7
A5 AVL -9
A7 CFLT -11
A9 BFLT -13
A11 AFLT -15
A13 CSTR -17
A15 BSTR -19
A17 ASTR P1-21
A36 PNS3 P2-9
A40 PADI -15
A41 PAD0 -17
A42 PAD2 -19
A43 PAD5 -21
A44 PAD7 -23
A45 PAD6 -25
A46 BBB,L -27
A47 BBH -29
A51 PIN CLK,L P2-31
A52 EVT P2-33
A53 FVT -35
A54 FVH -37
A55 FVL P2-39
B1 CVL P1-4
B2 CVH -6
B3 BVH -8
B5 AVT -12
B7 DFLT -14
B9 EFLT -16
B11 FFLT -18
B13 DSTR -22
B15 ESTR -24
B17 FSTR -26
B22 PNS5 -30
B24 PNS7 -34
B26 PNS6 P1-38
B28 PNS9 P2-4
B30 PNS8 -8
B32 PNS1 -12
B34 PNS4 P2-16
B38 PNS2 P2-22
B41 PAD3 -24
B43 PAD4 -26
B45 BBA -28
B47 BBM -30
B51 DVH -32
B52 DVL -34
B53 EVL -36
B54 DVT -38
B55 EVH P2-40
A16 GND P1-1
A18 GND P2-1
A20 GND P3-10
A22 GND -12
A28 GND -13
B14 GND -14
B16 GND -15
B18 GND P3-16
B20 GND
A38 +5V P3-1
A49 +5V -2
A50 +5V -3
B39 +5V -4
B40 +5V -6
B42 +5V P3-8
B44 +5V
B46 +5V
B48 +5V
B49 +5V
B50 +5V
SCHEMATIC DIAGRAM PANEL BOARD
L. DALES 9-17-80
RAM 9-19-80
9-25-86
GenRad
0100-2701/K
4/4

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	K	CHANGE PER ECO 335	7/12/79	J STEBL
	—	REVIEWED & CHANGES PER ENG. NOTEBOOK 1.0 0005	25 SEPT 80	RAM



QTY REQD	CODE IDENT	PART OR DWG NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

CONTRACT NO.

APPROVALS	DATE
	9-13-80

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

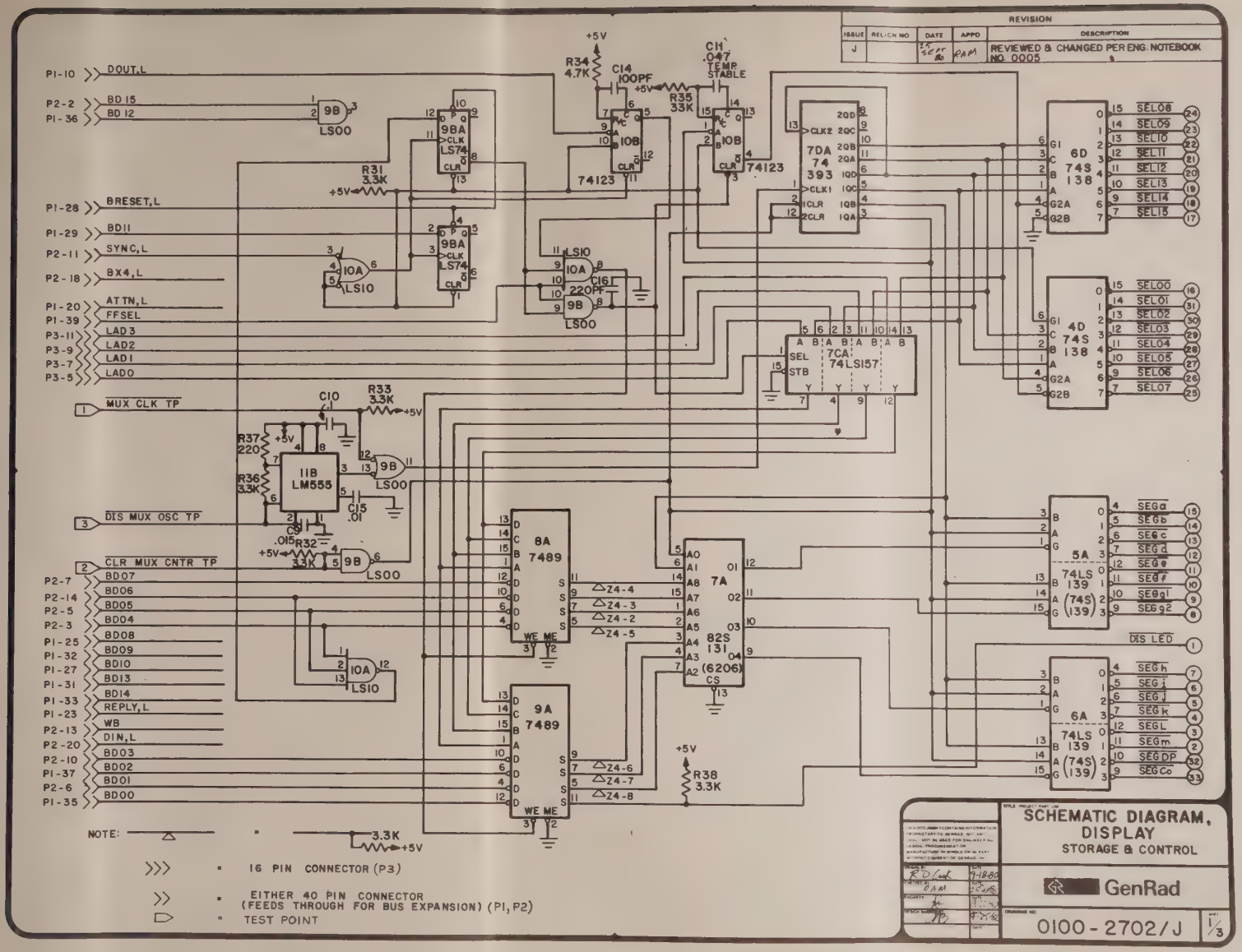
DO NOT SCALE DRAWING

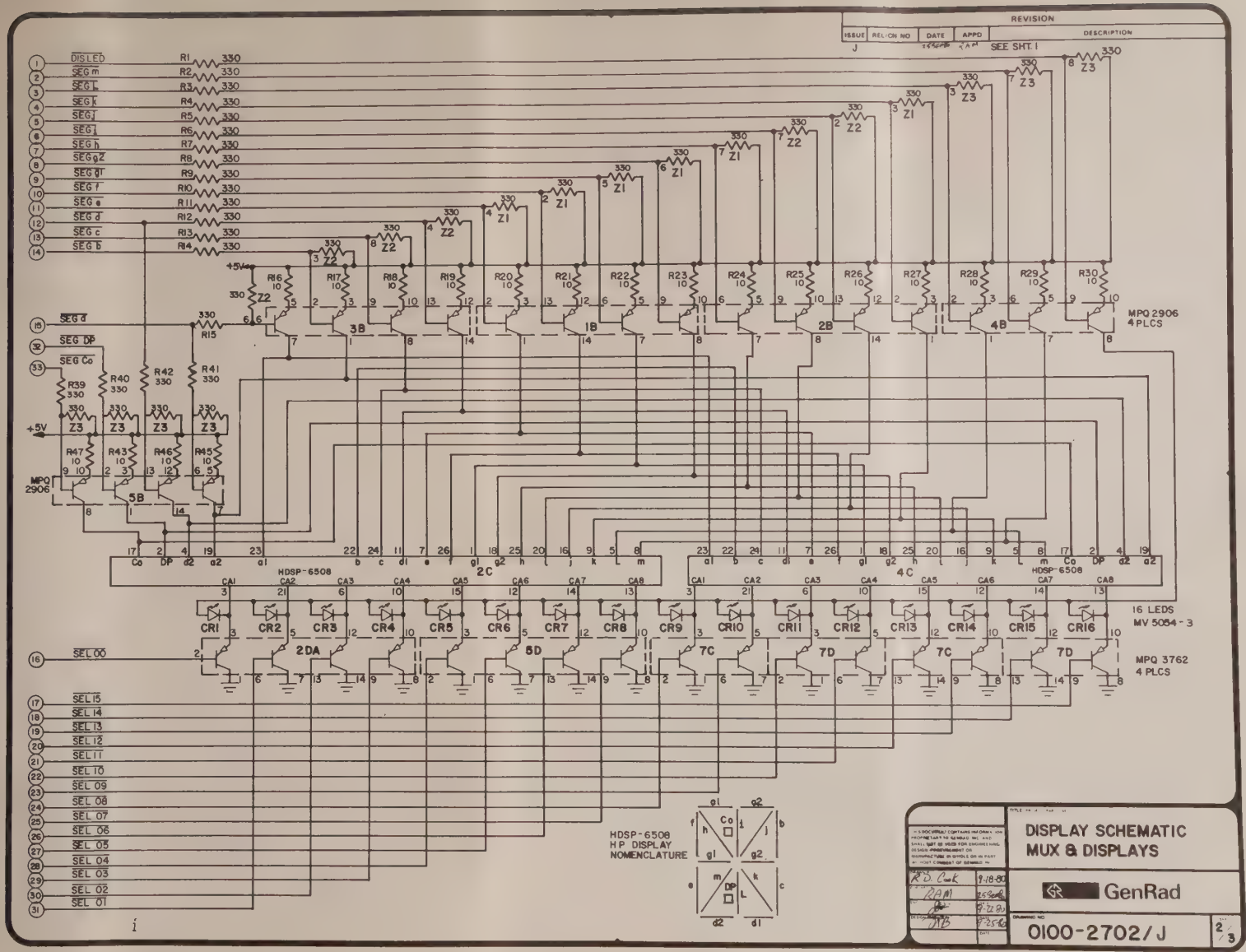
GenRad

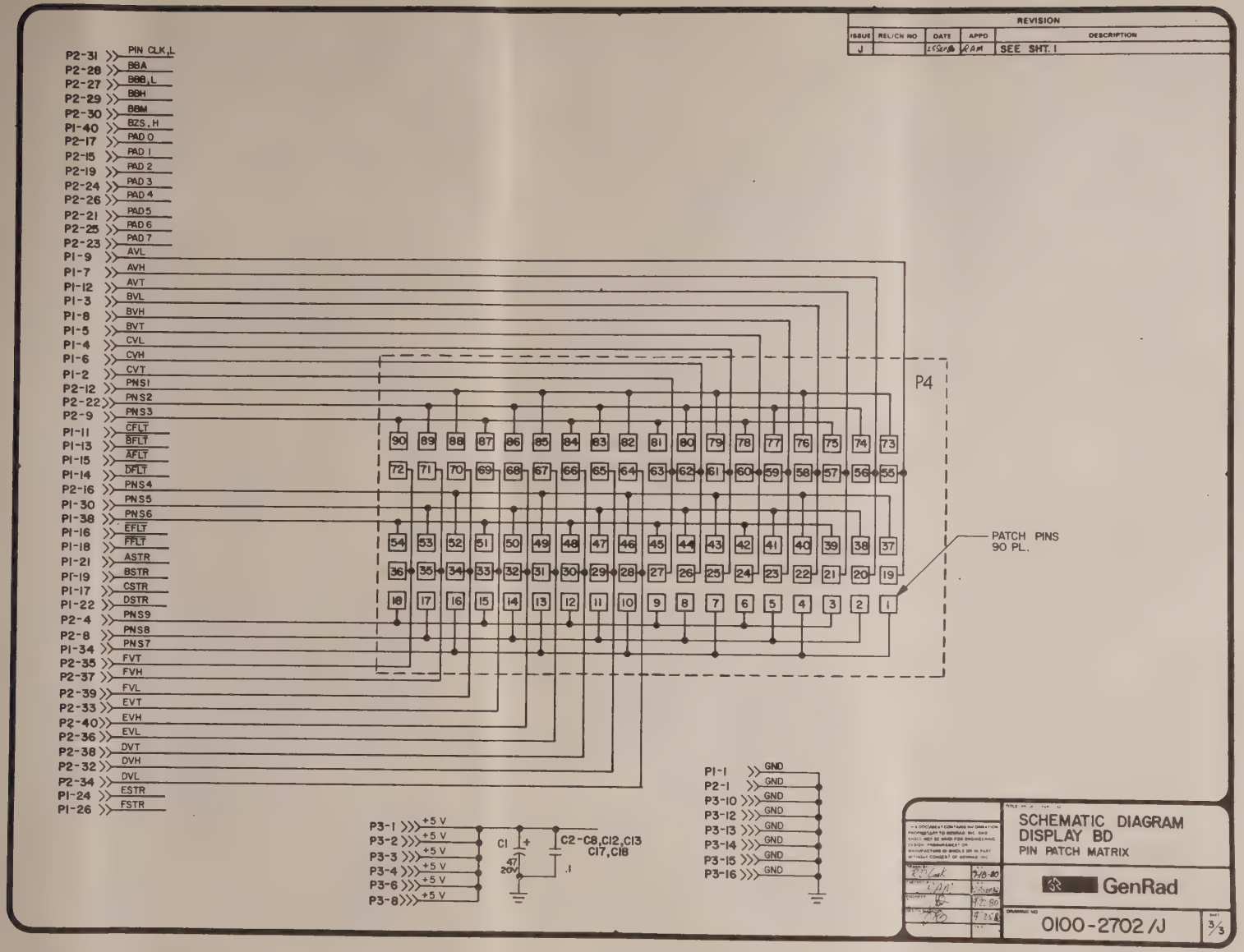
CIRCUIT CARD ASSEMBLY
DISPLAY BOARD

SIZE	CODE IDENT NO	DRAWING NO.	REV
D		0100-2702	K

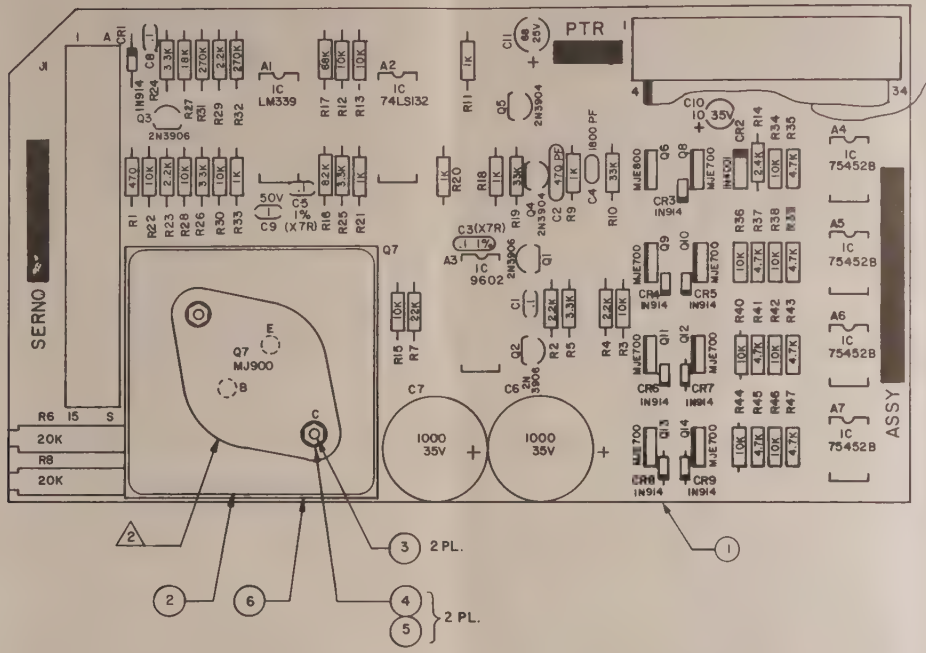
SCALE 2/1 SHEET 1 OF 1

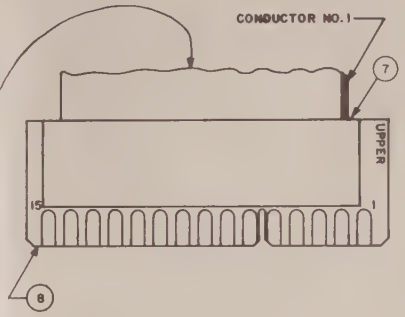

REVISION
ISSUE | RELEASE NO | DATE | APPD | DESCRIPTION
J | | 2.5 SEP 80 | RAM | REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005
P1-10 DOUT,L
P2-2 BD 15
P1-36 BD 12
P1-28 BRESET,L
P1-29 BDII
P2-11 SYNC,L
P2-18 BX4,L
P1-20 ATTN,L
P1-39 FFSEL
P3-11 LAD3
P3-9 LAD2
P3-7 LAD1
P3-5 LADO
1 MUX CLK TP
3 DIS MUX OSC TP
2 CLR MUX CNTR TP
P2-7 BD07
P2-14 BD06
P2-5 BD05
P2-3 BD04
P1-25 BD08
P1-32 BD09
P1-27 BD10
P1-31 BD13
P1-33 BD14
P1-23 REPLY,L
P2-13 WB
P2-20 DIN,L
P2-10 BD03
P1-37 BD02
P2-6 BD01
P1-35 BD00
+5V
R34 4.7K
C14 100PF
C11 .047 TEMP STABLE
R35 33K
R31 3.3K
74123
9B LS00
9A LS74
10A LS10
10B
C16 220PF
7DA 74 393
6D 74S 138
4D 74S 138
7CA 74LS157
SEL0 SEL1 SEL2 SEL3 SEL4 SEL5 SEL6 SEL7
C10 .1
R33 3.3K
R37 220
R36 3.3K
11B LM555
C15 .01
C9 .015
R32 3.3K
8A 7489
9A 7489
WE ME
Z4-4 Z4-3 Z4-2 Z4-5
Z4-6 Z4-7 Z4-8
7A 82S 131 (6206)
R38 3.3K
5A 74LS 139
6A 74LS 139
SEGa SEGb SEGc SEGd SEGe SEGf SEGg SEG 92
DIS LED
SEGh SEGj SEGk SEGL SEGm SEG DP SEG Co
NOTE: 3.3K +5V
>>> = 16 PIN CONNECTOR (P3)
>> = EITHER 40 PIN CONNECTOR (FEEDS THROUGH FOR BUS EXPANSION) (P1, P2)
= TEST POINT
SCHEMATIC DIAGRAM, DISPLAY
STORAGE & CONTROL
GenRad
0100-2702/J
1/3


REVISION
ISSUE | RELEASE NO | DATE | APPD | DESCRIPTION
J
SEE SHT. 1
DISLED
SEG m
SEG l
SEG k
SEG j
SEG i
SEG h
SEG g2
SEG g1
SEG f
SEG e
SEG d
SEG c
SEG b
SEG a
SEG DP
SEG Co
SEL 00
SEL 15
SEL 14
SEL 13
SEL 12
SEL 11
SEL 10
SEL 09
SEL 08
SEL 07
SEL 06
SEL 05
SEL 04
SEL 03
SEL 02
SEL 01
+5V
MPQ 2906
MPQ 2906 4 PLCS
HDSP-6508
HDSP-6508 HP DISPLAY NOMENCLATURE
16 LEDS MV 5084-3
MPQ 3762 4 PLCS
DISPLAY SCHEMATIC MUX & DISPLAYS
GenRad
0100-2702/J
2/3
R.S. Cook 9-18-80
RAM 9-24-80
9-25-80


REVISION
ISSUE | REL/CN NO | DATE | APPD | DESCRIPTION
J | | | RAM | SEE SHT. 1
P2-31 PIN CLK,L
P2-28 BBA
P2-27 BBB,L
P2-29 BBH
P2-30 BBM
P1-40 BZS,H
P2-17 PAD 0
P2-15 PAD 1
P2-19 PAD 2
P2-24 PAD 3
P2-26 PAD 4
P2-21 PAD 5
P2-25 PAD 6
P2-23 PAD 7
P1-9 AVL
P1-7 AVH
P1-12 AVT
P1-3 BVL
P1-8 BVH
P1-5 BVT
P1-4 CVL
P1-6 CVH
P1-2 CVT
P2-12 PNS1
P2-22 PNS2
P2-9 PNS3
P1-11 CFLT
P1-13 BFLT
P1-15 AFLT
P1-14 DFLT
P2-16 PNS4
P1-30 PNS5
P1-38 PNS6
P1-16 EFLT
P1-18 FFLT
P1-21 ASTR
P1-19 BSTR
P1-17 CSTR
P1-22 DSTR
P2-4 PNS9
P2-8 PNS8
P1-34 PNS7
P2-35 FVT
P2-37 FVH
P2-39 FVL
P2-33 EVT
P2-40 EVH
P2-36 EVL
P2-38 DVT
P2-32 DVH
P2-34 DVL
P1-24 ESTR
P1-26 FSTR
P4
90 89 88 87 86 85 84 83 82 81 80 79 78 77 76 75 74 73
72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55
54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37
36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
PATCH PINS
90 PL.
P3-1 +5 V
P3-2 +5 V
P3-3 +5 V
P3-4 +5 V
P3-6 +5 V
P3-8 +5 V
C1
47
20V
C2-C8,C12,C13
C17,C18
.1
P1-1 GND
P2-1 GND
P3-10 GND
P3-12 GND
P3-13 GND
P3-14 GND
P3-15 GND
P3-16 GND
SCHEMATIC DIAGRAM
DISPLAY BD
PIN PATCH MATRIX
GenRad
0100-2702/J
3/3

REVISION				
ISSUE	REL CN NO	DATE	APPD	DESCRIPTION
C		11-14-78		REVISED PER ECO 189
-		12-12-79		REDRAWN WITHOUT CHANGE
D		7-30-80	BCW	REV PER ECO 439
D		20 SEPT 80	RAM	REVIEWED & CHANGED PER ENG NOTEBOOK NO. 0006





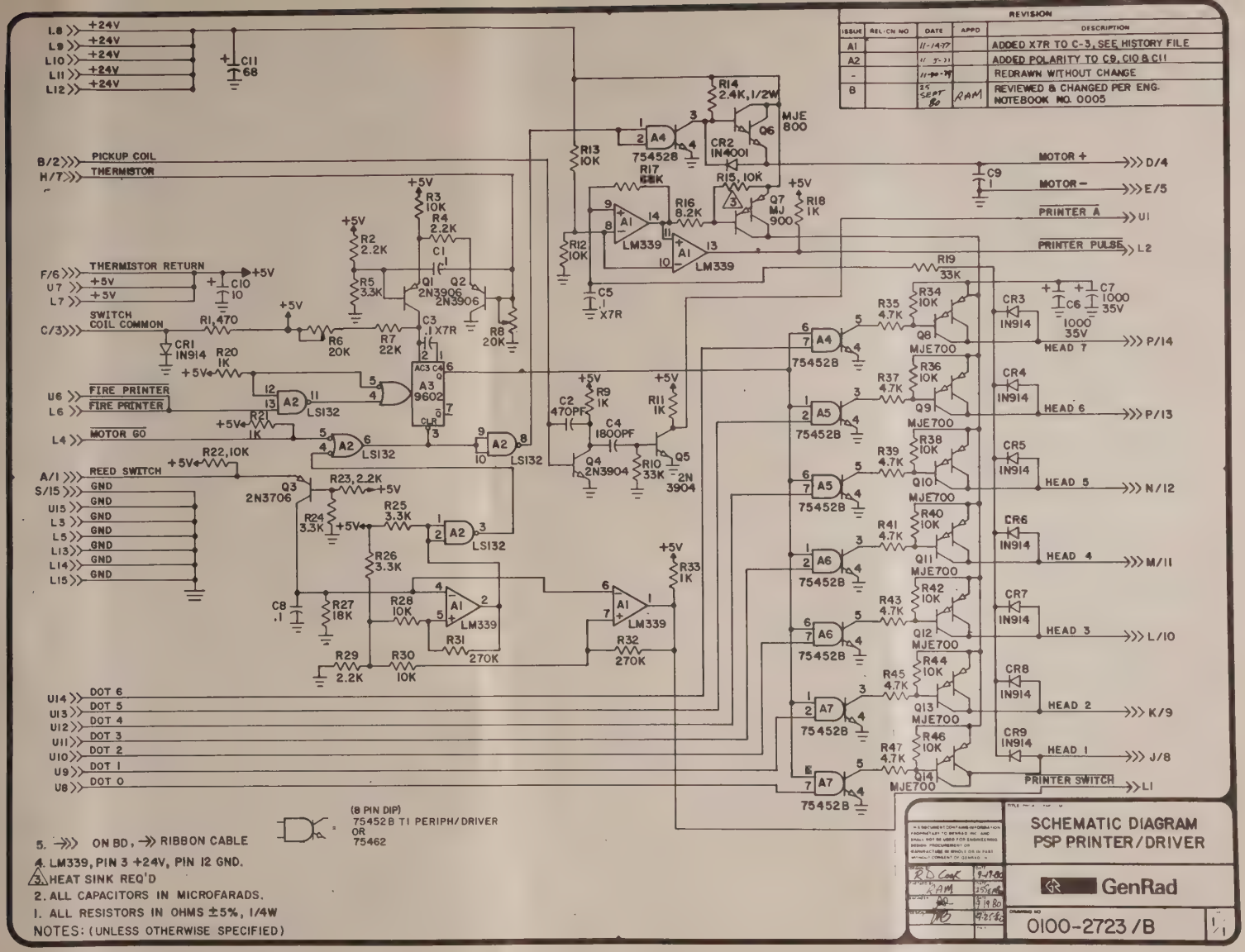
NOTES:

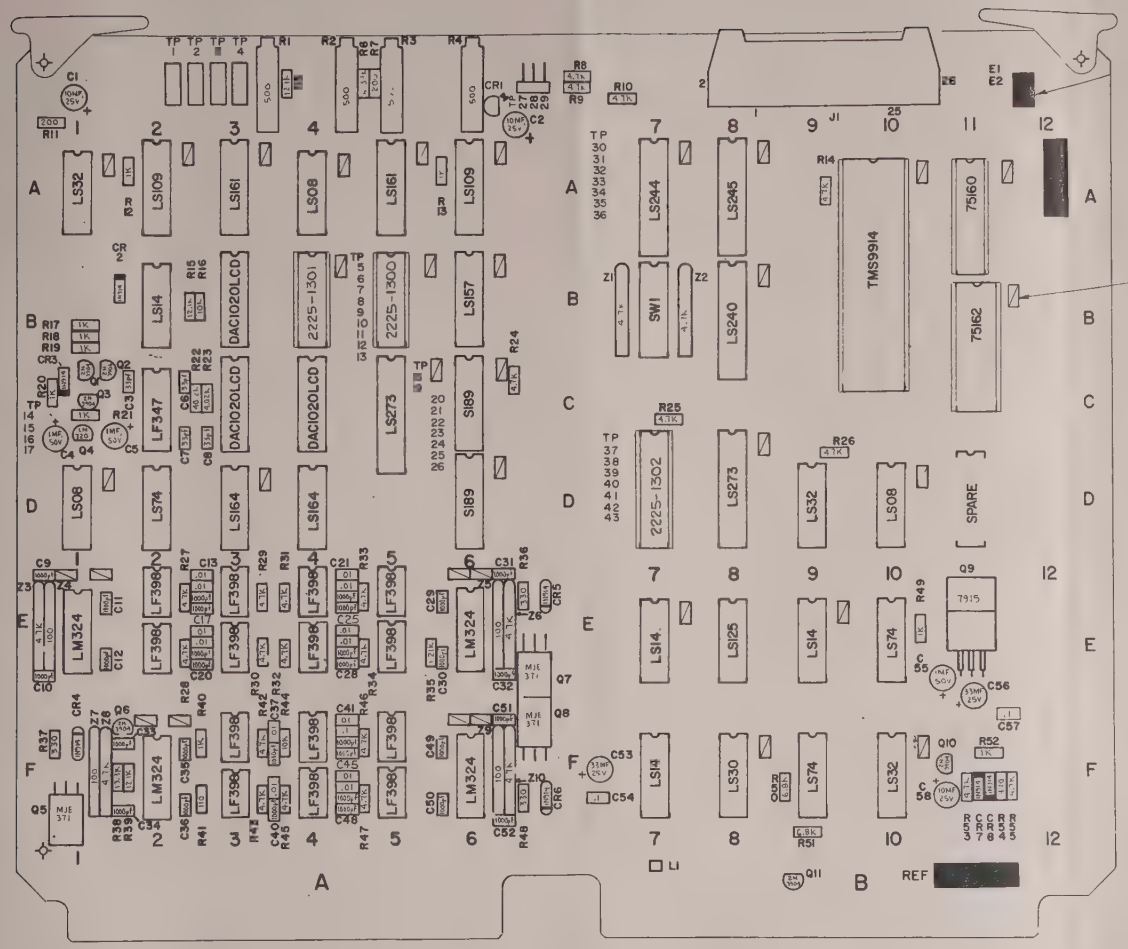
1. INSTALL PADDLE BOARD & CABLE ASSY, ITEM 7 & 8, AND ALSO Q7, C7, C8. AFTER WAVE SOLDERING.
2. PUT HEAT SINK COMPOUND, ITEM 9, ON BOTTOM OF Q7 BEFORE INSTALLATION.
3. ALL RESISTOR ARE IN OHMS.
4. ALL CAPACITORS ARE IN MICROFARADS.

CIRCUIT CARD ASSY
PSP PRINTER / DRIVER

GenRad

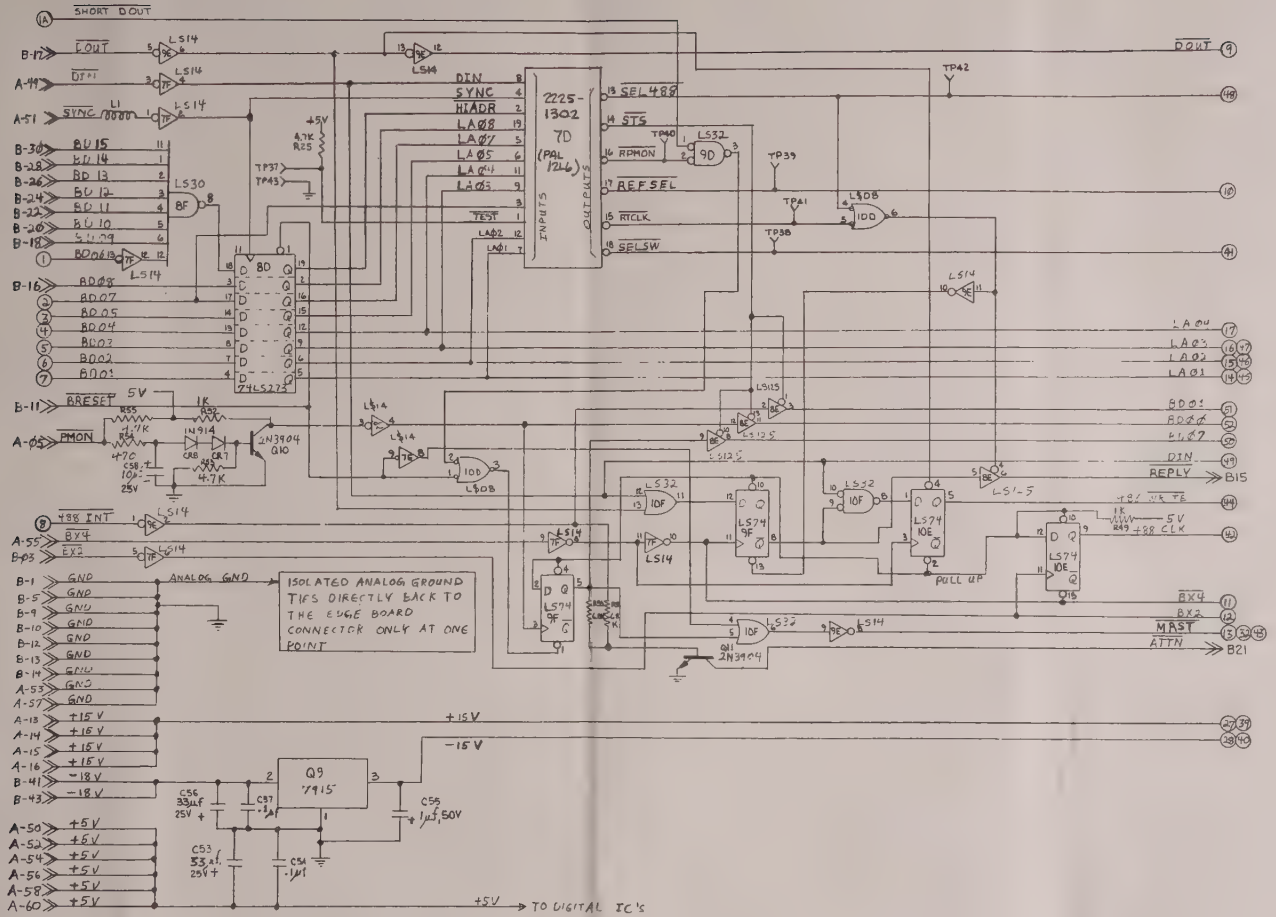
0100-2723 / D


REVISION
ISSUE | REL'CN NO | DATE | APPD | DESCRIPTION
A1 | | 11-14-77 | | ADDED X7R TO C-3, SEE HISTORY FILE
A2 | | 11-30-77 | | ADDED POLARITY TO C9, C10 & C11
- | | 11-30-79 | | REDRAWN WITHOUT CHANGE
B | | 25 SEPT 80 | RAM | REVIEWED & CHANGED PER ENG. NOTEBOOK NO. 0005
SCHEMATIC DIAGRAM
PSP PRINTER/DRIVER
GenRad
0100-2723 /B
PICKUP COIL
THERMISTOR
THERMISTOR RETURN
SWITCH COMMON
FIRE PRINTER
FIRE PRINTER
MOTOR GO
REED SWITCH
MOTOR +
MOTOR −
PRINTER A
PRINTER PULSE
PRINTER SWITCH
HEAD 7
HEAD 6
HEAD 5
HEAD 4
HEAD 3
HEAD 2
HEAD 1
DOT 6
DOT 5
DOT 4
DOT 3
DOT 2
DOT 1
DOT 0
LM339
LSI32
MJE800
MJE700
2N3906
2N3904
IN914
IN4001
75452B
9602
(8 PIN DIP)
75452B TI PERIPH/DRIVER
OR
75462
5. →» ON BD, →» RIBBON CABLE
4. LM339, PIN 3 +24V, PIN 12 GND.
3. HEAT SINK REQ'D
2. ALL CAPACITORS IN MICROFARADS.
1. ALL RESISTORS IN OHMS ±5%, 1/4W
NOTES: (UNLESS OTHERWISE SPECIFIED)



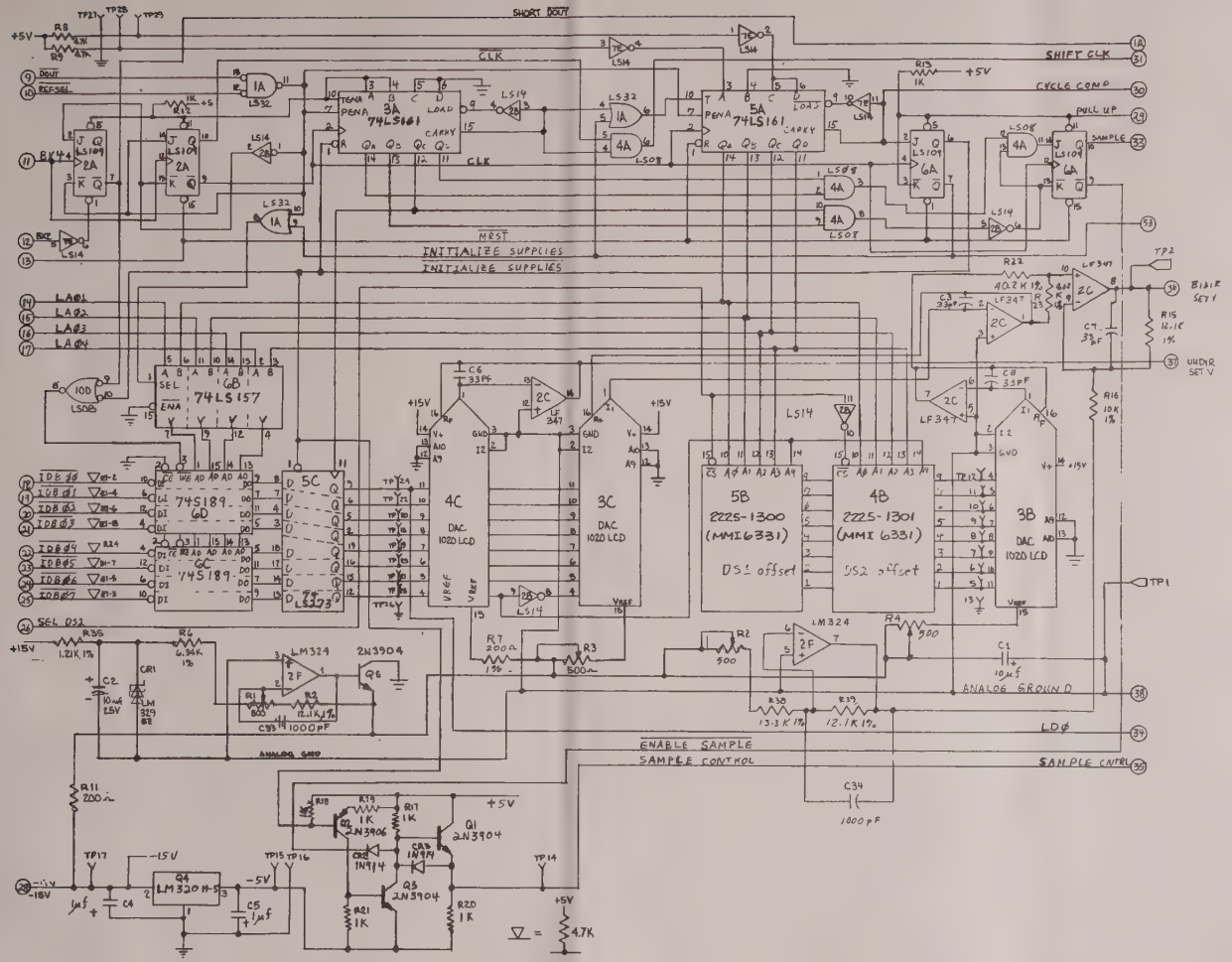
CIRCUIT CARD ASSY
REFERENCE - IEEE

2225-2703 Rev. A (Sheet 1 of 1)



SCHEMATIC DIAGRAM
REFERENCE BOARD
(BOARD SELECT LOGIC)

2225-2703 Rev. A (Sheet 1 of 4)



SCHEMATIC DIAGRAM
REFERENCE BOARD
(MULTIPLEXED REF.)

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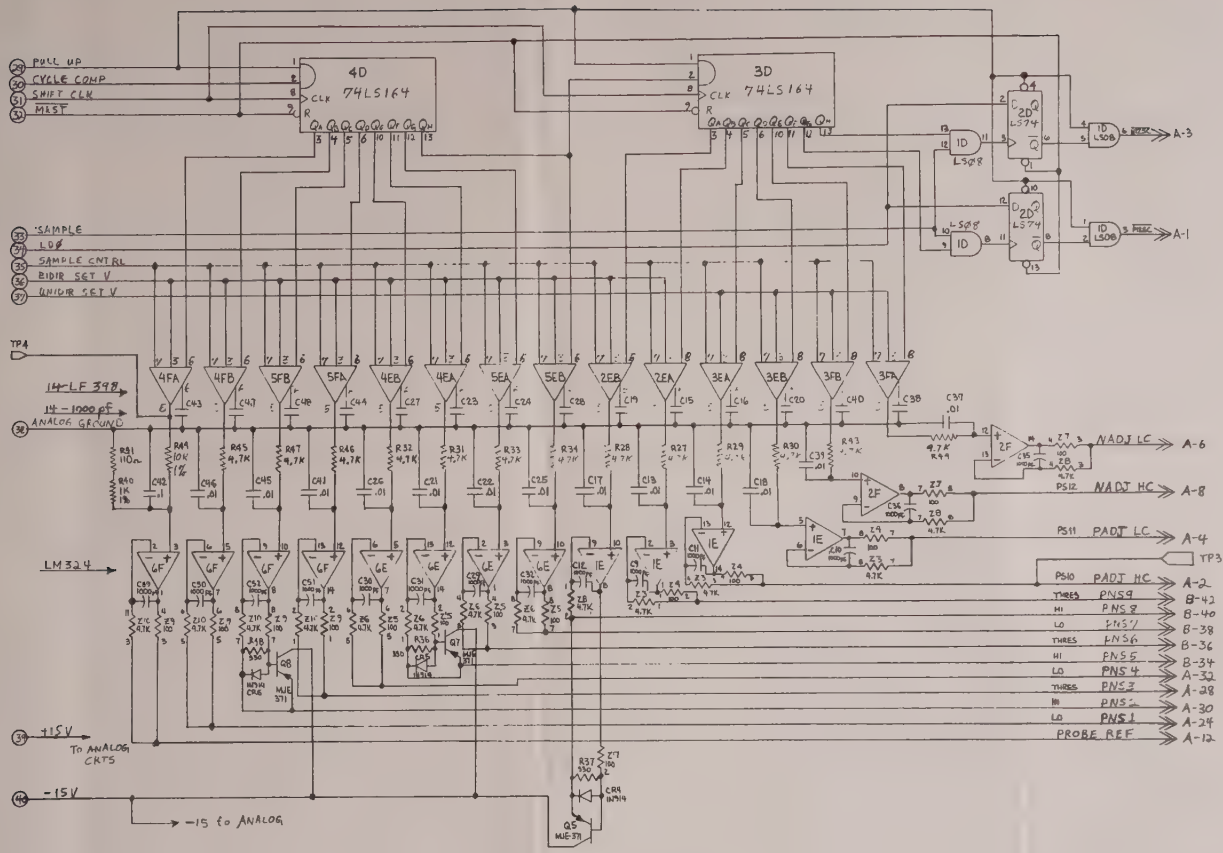

SCHEMATIC DIAGRAM
REFERENCE BOARD
(ANALOG OUTPUT DRIVERS)

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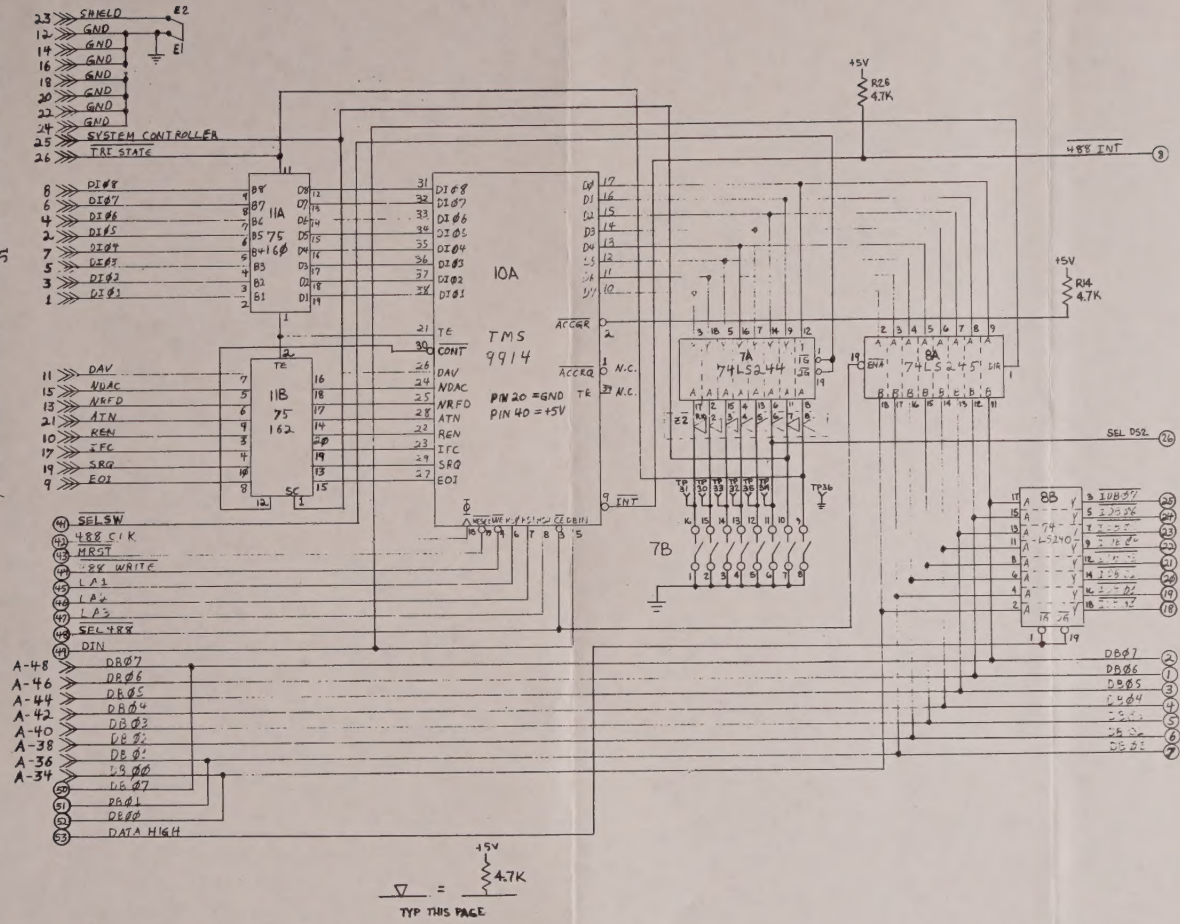

SCHEMATIC DIAGRAM
REFERENCE BOARD
(IEEE-48 INTERFACE)

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